EPC®-1316 User's Guide

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⚠ DANGER

If you plan to connect a floppy drive, you must use a RadiSys EXP-FDM (Floppy Disk Module).

Connecting a standard floppy drive can create a fire hazard and may damage or destroy the EPC-1316 baseboard, MSIO carrier board, MSF option board, EXP-FDM, or cable.

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Before you begin

This manual provides detailed hardware reference information for OEMs, system integrators, and others who use the EPC-1316 as a component of their VMEbus systems. It also explains how to install the EPC-1316, and configure the BIOS and the board configuration options.

This manual assumes that you are familiar with both PC systems based on the Intel x86 architecture and with VMEbus architecture.

Guide contents

Chapters

Chapter		Description
11	Overview	Provides an introduction to the EPC-1316, a brief description of the features provided, and specifications.
2	Configuration and installation	Covers the details of installing the EPC-1316 in a VME mainframe.
3	BIOS configuration	Describes the process of BIOS configuration using the built-in BIOS setup menus.
4	Theory of operation	Describes how the components of the EPC-1316 operate to provide a PCI/VMEbus compatible embedded computer with standard PC peripherals and PCI, and VME interfaces.
5	Programming the VMEbus interface	Describes initializing and programming the VMEbus interface using the system BIOS and the Tundra Universe II† PCI-VME bridge chip.

Appendices

Appendix		Description
A	Chipset and I/O map	Maps the addresses used for I/O and by the chipset registers.
B	Interrupts	Shows the DMA channel and IRQ assignments to the peripherals supported by the EPC-1316.
C	Connectors	Details the location, form, and pin-outs of the connectors used in the EPC-1316.
D	Registers	Maps the address space used by EPC-1316 and VMEbus registers.
E	Error messages and diagnosis	Provides explanations of common error messages and start-up codes.

Appendix		Description
F	MSIO Carrier Board	Describes how to configure and use the MSIO option board.
G	MSF option board	Describes how to and use the MSF option board.
H	Flash disk module	Describes how to install, configure, and use the optional Flash module.
I	PMC modules	Describes how to install, configure, and use optional PMC modules.
J	Installing and configuring RomPilot	Describes how to install, configure, and enable a RomPilot image on a server and the Management Workstation software on a client.
K	Re-programming the flash chip	Explains how to update or recover your system BIOS, Flash Boot Device (FBD), and Boot Block by re-programming the Flash chip on the main board.
L	Glossary	Defines terms used in this guide.

Notational conventions

This manual uses the following conventions:

- `Screen text and syntax strings appear in this font.`
- All numbers are decimal unless otherwise stated.
- Bit 0 is the low-order bit. If a bit is set to 1, the associated description is true unless otherwise stated.

Notes indicate important information about the product.

Tips indicate alternate techniques or procedures that you can use to save time or better understand the product.

The globe indicates a World Wide Web address.

The book indicates a book or file.

ESD cautions indicate situations that *may* cause damage to hardware via electro-static discharge (ESD).

Cautions indicate potentially hazardous situations which, if not avoided, may result in minor or moderate injury, or damage to data or hardware. It may also alert you about unsafe practices.

Warnings indicate potentially hazardous situations which, if not avoided, can result in death or serious injury.

Danger indicates imminently hazardous situations which, if not avoided, will result in death or serious injury.

Where to get more information

About the EPC-1316

You can find out more about the EPC-1316 from these sources:

- **World Wide Web**: RadiSys maintains an active site on the World Wide Web. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, and technical support information. You can also send e-mail to RadiSys using the web site.

  When sending e-mail for technical support, please include information about both the hardware and software, plus a detailed description of the problem, including how to reproduce it.

  To access the RadiSys web site, enter this URL in your web browser:

  `http://www.radisys.com`

  Requests for sales, service, and technical support information receive prompt response.

- **Other**: If you purchased your RadiSys product from a third-party vendor, you can contact that vendor for service and support.

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1 Overview

The EPC®-1316 is a Pentium† III-based PC-compatible computer designed to interface to the VME backplane bus. The electronics are comprised of a 6U size I/O base board. The board comes in single-slot (6U I/O baseboard) and double-slot (6U I/O baseboard plus option card) configurations.

The EPC-1316 supports DOS 6.22, VxWorks, and Microsoft† Windows† 95, Windows 98, Windows NT† V4 and Windows 2000. The system is year-2000 ready.

The EPC-1316 also supports EPConnect, a C/C++ programming interface to the Microsoft Windows NT API. For more information about EPConnect, see the *EPConnect for Windows NT/4.0 Programmer's Reference Guide*, available from Radisys.

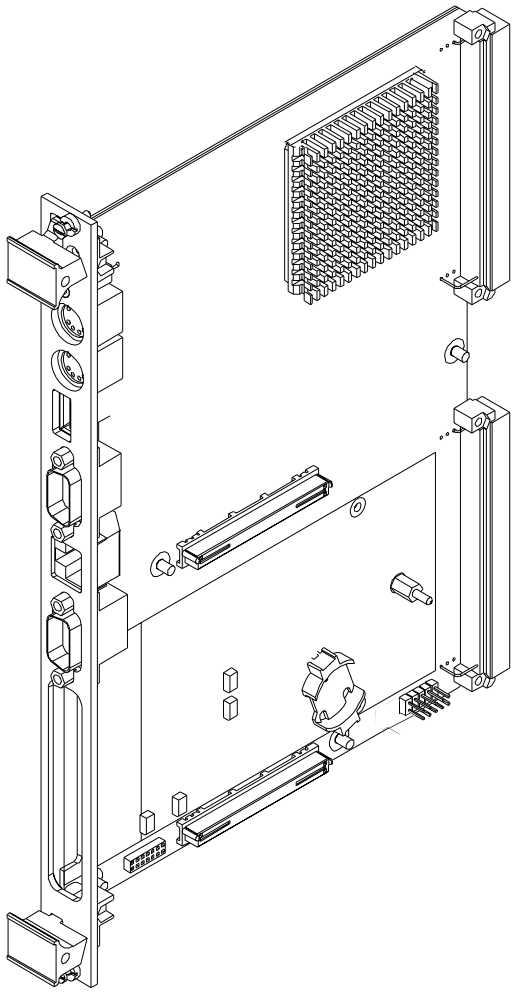

Figure 1-1. The EPC-1316, shown with no options

The EPC-1316 can be ordered in these configurations:

Configuration	Options	Description
EPC-1316	You can order this configuration with: • No options. • A Flash disk module.	The Flash disk module is a 64-Mbyte PCI Mezzanine card that conforms to IEEE P1386.1. Available only for EPC-1316s that do not include an option card or PMC card. For more information about PMC modules, see *Appendix I, PMC modules*.
EPC-1316 + MSIO Carrier Board[1]	You can order this configuration with: • A hard disk drive. • A Flash drive.	The EPC-1316 board plus a mass storage and I/O expansion board (MSIO) which provides SCSI, LPT, floppy drive, and IDE (primary) interfaces, as well as one RS-232/RS-485 serial port. For more information about the Carrier board, see *Appendix F, MSIO Carrier Board*.
EPC-1316 + MSF option board[1]	You can order this configuration with: • A hard disk drive. • A Flash drive.	The EPC-1316 board plus an MSF (Multi-Serial Feature) card that provides secondary storage and multiple I/O functions. For more information about the Carrier board, see *Appendix G, MSF option board*.

1 Available only for EPC-1316 boards not fitted with the Flash disk module option.

The EPC-1316 can be fitted with a PMC module, a PCI Mezzanine card that conforms to IEEE P1386.1. Available only for EPC-1316s that do not include the Flash disk module. For more information about PMC modules, see *Appendix I, PMC modules*.

The EPC-1316 does not require a RadiSys-manufactured PMC. The EPC-1316 can accept most PMC types excluding those that either require a disk BIOS in the EPC or do not fit by form factor.

Feature summary

Component	Features
Processor	• BGA2 processor. • 400 MHz mobile Pentium III. • 256KB of L2 cache, running at full processor speed.
Main memory	• Two 144-pin PC100 SODIMM sockets. • Supports up to 256 MB synchronous DRAM (SDRAM).
Intel North Bridge 443BX	• Host Bus to 32 bit, 33 MHz PCI bridge. • SDRAM support without ECC.
Intel South Bridge 82371EB PCI ISA IDE Xcelerator (PIIX4E)	• PCI to ISA bridge. • Two independent EIDE channels. • Single channel USB support. • Integrated RTC with external battery backup.
National PC87309-ICK-VLJ Super I/O	• Two serial ports (one provided by MSIO). • One parallel port (only with MSIO). • One PS/2 keyboard port. • One PS/2 mouse port. • Two floppy drives (one supported by MSIO, one provided via P2 connector).
Video graphics	• Chips and Technology 69030 64-bit GUI and video-accelerated controller. • 4 MB of video memory integrated into the video controller.

Other features	• Phoenix†-based PC BIOS with Flash update capability from floppy. Writes to the BIOS Flash are controlled by software that uses registers in the chipset. Installing a jumper can force updates to the BIOS Flash.
	• Remote management capability, using RomPilot software.
	• Full 32-bit VME bus interface with P1 and P2 connectors which includes these features:
	  • Master control in the A16/A24/A32 address spaces for D08, D16, and D32 data widths.
	  • D64/D32/D16/D08 slave control in the A32/A24 address space for dual port DRAM.
	  • D16 slave control in the A16 address space for dual-ported VXI configuration and message-passing registers.
	  • VME-bus arbiter, SYSCLOCK driver, and bus time-out.
	  • Generate and respond to all seven VME-bus interrupts.
	• One IEEE P1386.1 PCI Mezzanine Card site via front panel.
	• PCI-based Ethernet 10/100 BASE-T interface with an RJ45 connector.
	• Watchdog timer. This device can, upon proper configuration, generate a VMEbus SYSFAIL signal and either halt or perform a warm reboot of the processor. The timer is implemented as a software-retriggerable one-shot, with a programmable reset interval ranging from 128 ms to 8.2 seconds.

VMEbus

The Universe† chip (the Tundra† Universe II VME/PCI Bridge chip with enhancements for multiprocessor environments) controls the VMEbus. The next sections cover system controller functions, the VMEbus master interface, and the VMEbus extended register set.

System controller functions

The Universe chip allows the EPC-1316 to provide full VME Slot-1 arbitration functions. When enabled, these functions include priority and round-robin bus arbitration, IACK and bus grant daisy-chain driving, SYSRESET and SYSCLK generation and bus time-out detection. ROR (release-on-request), RWD (release when done) or a fair-requester, RONR (release-on-no-request) bus release mechanism is software selectable.

VMEbus master interface

The VMEbus master interface provides a full 64/32-bit data path to the 16-, 24-, and 32-bit address spaces of the VMEbus. The bus interface is designed with a minimum number of state registers, which maximizes performance in a multitasking or interrupt-driven environment.

Programmable hardware byte-swapping provides ease of communication with other processor architectures that may share the VMEbus. All the VMEbus address spaces can be addressed from both protected-mode and real-mode operating systems.

The EPC-1316 can generate or respond to all seven standard VMEbus interrupts, and can also receive as interrupts the VMEbus signals ACFAIL, BERR, and SYSFAIL. When it generates interrupts, the EPC-1316 implements 16-bit IACK cycles.

VMEbus extended register set

As an extension to the VMEbus interface, the EPC-1316 implements the set of VXIbus (IEEE 1155-1992) standard multiprocessor support registers in the A16 space.

These registers provide a set of standard identification, status, control and communication functions that are useful in multiprocessor environments. They allow dynamic system configuration by providing for board identification, and provide well-defined multi-processor communications channels and protocols.

The EPC-1316 includes a complete set of VXIbus-defined message-based device registers. These registers are implemented in a proprietary gate array and mapped into the VMEbus A16 address space and include a device-type identifier register, bus status and control registers, and a register-based message passing facility.

PCI Mezzanine card interface

The PMC card interface, which resides on the PCI bus as device 3 (AD14), has interrupt and bus master capability.

The signal connections are for a 32-bit PCI revision 2.1 compliant interface and do not have the 64-bit data path connector.

There is no provision for additional I/O signals via the PMC connectors.

For information about inserting PMC cards in this interface, see *Appendix I, PMC modules*.

Specifications

Environmental specifications

Table 1-1. EPC-1316 environmental specifications

Characteristic	State	Value
Temperature	Operating	0 to 55°C at point of entry of forced air derated 2°C per 1000 ft. (300 m) over 6600 ft. (2000 m)
	Storage	–40°C +85°C
Humidity	Operating	5% to 95% noncondensing
	Storage	5% to 95% noncondensing
Altitude	Operating	0–10,000 ft (3000 m)
	Storage	0–40,000 ft (12,000 m)
Vibration (excluding hard drive)	Operating	2.5 g acceleration over 5–300 Hz sine wave (P-P), 1 oct/min sine sweep
	Storage	5 g acceleration over 5–2 kHz sine wave (P-P), 1 oct/min sine sweep
Shock (excluding hardd drive)	Operating	30 g, 11 ms duration, half-sine shock pulse
	Storage	50 g, 11 ms duration, half-sine shock pulse
Airflow		200 LFM (linear feet per minute)

Power supply requirement specifications

Table 1-2. EPC-1316 power supply specifications

Characteristic	Value
Current	+5V @ 4–7A (options excluded)
	+12V @ 350 mA (options excluded)
	–12V @ 50 mA (options excluded)

Additional specifications

Table 1-3. Additional EPC-1316 specifications

Characteristic	Value
Mechanical	Standard VME 6U card
Weight	2.7 lb. (1.3 kg) with PMC site unpopulated
Dimensions	One-slot 6U VMEbus model
Safety	UL 1950 73/23/EECLow-Voltage Directive using EN 60950
EMC	RadiSys embedded computers are designed with good EMC practices as intended in “The Council of The European Communities EMC Compatibility Directive” (89/336/EEC). RadiSys currently follows these standards: EN55022 Limits and Methods, ITE EN55024 Immunity, ITE (where applicable)

Table 1-3. Additional EPC-1316 specifications

Characteristic	Value	
VME	Master address	A16, A24, A32
	Master transfer	D08(EO), D16, D32, D64, RMW
	Slave address	A16
	Slave transfer	D08(EO), D16, RMW
	Interrupter	I(1–7)
	Interrupt handler	D08(O),D16 IH(1–7)
	Requester	ROR, RONR, RWD
	Arbiter	RRS, PRI
	System controller	SYSCLK, IACK and bus grant daisy chain drivers, and bus time-out error (BERR)
VXI	Device type	Message based
	Protocols	Servant/commander/master/interrupter
	Manufacturer code	4076 RadiSys Corporation
	Model code	101Fh (if configured for slot 0) 111Fh (if configured for other than slot 0)

2 Configuration and installation

This chapter explains how to install and configure the EPC-1316. To install or configure options for the EPC-1316, see the appropriate appendix:

- **MSIO Carrier Board**: see *Appendix F, MSIO Carrier Board*.
- **MSF option board**: see *Appendix G, MSF option board*.
- **Flash disk module**: see *Appendix H, Flash disk module*.
- **PMC modules**: see *Appendix I, PMC modules*.

When reading this file online, you can immediately view information about any installation topic by placing the mouse cursor over a connector name and clicking:

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Avoid causing ESD damage:

- Remove modules from their antistatic bags only in a static-free environment.
- Perform the installation process (described later in this chapter) only in a static-free environment.
- During the installation process, ensure that power to your system is off. The EPC-1316 is not designed to be inserted or removed while the chassis is powered up.
- During external cable installation, ensure that the cables are not active. The EPC-1316 is not designed for hot insertion of any interface.

The EPC-1316 modules, like most other electronic devices, are susceptible to electrostatic discharge (ESD) damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

Configuring the EPC-1316

Slot-1 functionality

Every VMEbus system must have a System (Slot-1) Controller. The Slot-1 controller provides the following functionality:

- Serves as the bus arbiter (priority or round-robin)
- Drives the 16 MHz SYSCLK signal
- Starts the IACK and bus grant daisy chain
- Provides bus timeout error (BERR) function

When inserted in Slot 1, the EPC-1316 is automatically configured to provide standard VMEbus Slot-1 functionality. The Slot-1 configuration option is enabled automatically by detecting the VMEbus ~BG3IN signal if the board is the system controller (Slot-1). If ~BG3IN is sampled low immediately after reset, the EPC-1316 is installed in Slot-1 and becomes the system controller.

The EPC-1316 always powers up in non-system controller mode and samples ~BG3IN to determine whether or not it is the system controller. When configured as the Slot-1 controller, the EPC-1316 performs all the standard VMEbus system control functions.

Selecting the EPC-1316 slot location

To maintain fire and electric shock safety standards, install the EPC-1316 in a safety-approved VMEbus enclosure compliant with EN-60950.

When deciding where to position the EPC-1316 in the chassis, determine whether the EPC-1316 will function as system controller. If so, it must be placed in slot 1. The VMEbus specification, Rule 3.3, states that the Slot-1 controller must be in slot 1. All other boards must be to the right of the Slot-1 controller.

The EPC-1316 plus any option can be considered together as a single subsystem. Check the total power requirements against the power supply ratings of your VMEbus system and the other modules to ensure that the power supply can handle the total power required.

Once you determine the EPC-1316 subsystem physical location in the chassis, the VMEbus backplane must be jumpered appropriately, as described in the following section.

Installing the VMEbus backplane jumper

The VMEbus propagates four bus grant signals (BG0–BG3) and one interrupt acknowledge signal (IACK) via daisy-chain lines. Per the VMEbus specifications, all boards (that plug into the backplane) must handle these signals correctly. All slots that do not have a board plugged into the backplane (for example, empty slots), need to be jumpered to allow the signals to pass through to other boards in the system.

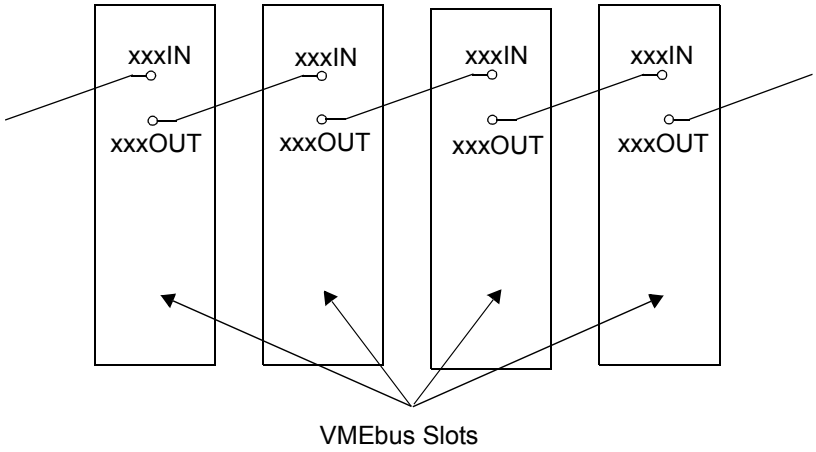


Figure 2-1. Daisy-chain signal concept

The daisy-chain signal concept is shown in the above figure. The Slot-1 controller initiates each daisy-chain signal. Each VMEbus slot to the right of the Slot-1 controller, as viewed from the front, must pass through each of the daisy-chained signals. For each VMEbus slot, the xxxIn pin must be connected to its corresponding xxxOut pin either through the board in that slot or by jumper. For example, BG0In–BG3In to BG0Out–BG3Out, respectively; IackIn to IackOut. (Boards that meet VMEbus specifications correctly handle the signals and do not need backplane jumpers. However, many early designs may not handle any of these signals.)

Check the manual for each board to be installed to determine if these signals are passed through correctly. If these signals are not handled correctly by the board in question or if the VMEbus slot is empty, all (or some) of these signals must be jumpered to the next location in the daisy-chain. See Figure 2-2 and Figure 2-3 on the following pages.

Setting jumpers on the backplane

The EPC-1316's leftmost slot does not require any jumpers. All other slots occupied by the subsystem require that all five jumpers be installed.

Once you determine where the jumpers need to be, you must determine how to add jumpers to your particular backplane. Different backplane manufacturers handle this in different ways: some provide stake pins or wirewrap pins on the rear of the backplane while others provide pins on the front of the backplane. These stake pins can be located in several different places.

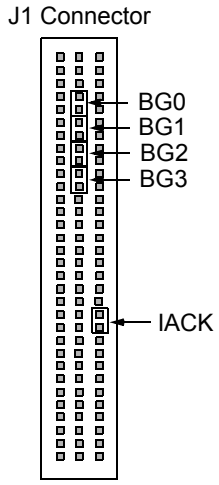


Figure 2-2. VMEbus jumpers on rear wirewrap pins

If the stake pins are on the rear of the backplane, the most common location is in the middle of the J1 connector as shown in Figure 2-2. The connector may have wire-wrap tails on all pins, or just on the bus-grant and IACK pins.

Stake pins (front or rear) can also be located adjacent to the slot being jumpered as shown in Figure 2-3. Typically, the stake pins are located between the jumpered slot and the next lower-numbered slot (for example, jumpers for Slot 6 are located adjacent to Slot 6, between Slots 5 and 6).

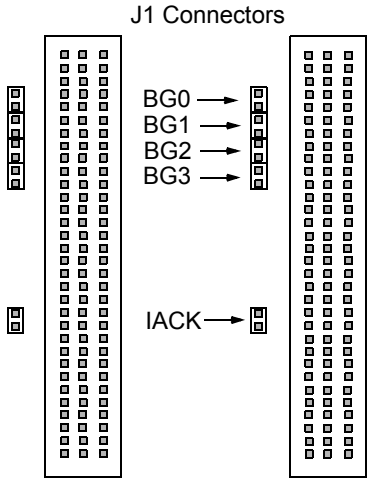


Figure 2-3. VMEbus jumpers on front stake pins

Consult your VMEbus chassis reference manual or contact the chassis manufacturer if you are unsure where to jumper your particular system.

Setting jumpers on the boards

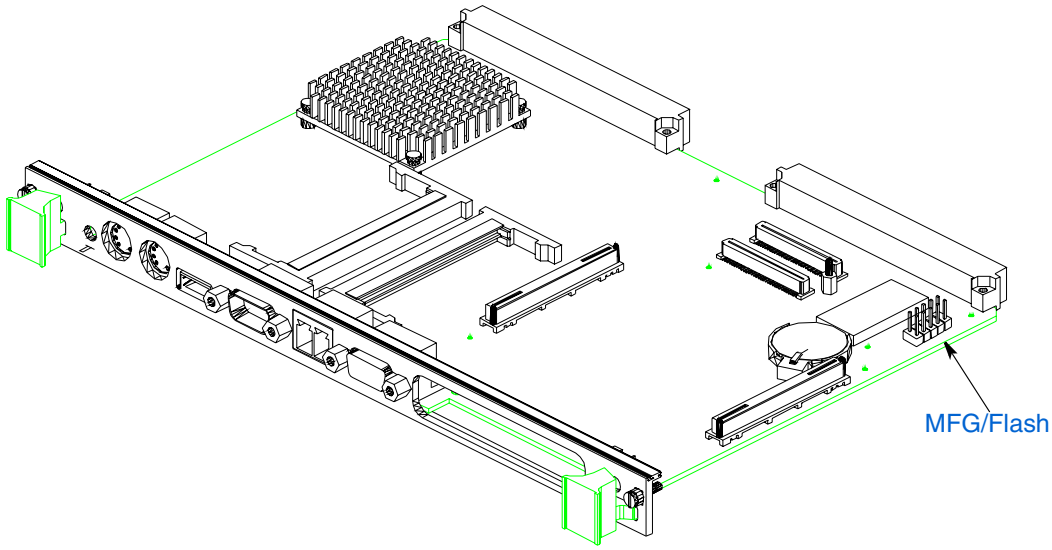


Figure 2-4. EPC-1316 assembly: jumper locations

Jumper pins are labeled from the point of view of looking at the front of the connector.

MFG/Flash

The EPC-1316 provides a 2x6-pin header used for for testing purposes and to re-program the Flash chip. For detailed information about re-programming the flash chip, see *Appendix K, Re-programming the flash chip*.

Flash jumper settings are typically used during manufacturing for configuration and are included here only for reference.

Figure 2-5. Flash jumper settings

Inserting the EPC-1316

You install the EPC-1316 on the VMEbus backplane. Before installation, ensure that all options are installed on the EPC-1316 as described in *Maintaining and upgrading the EPC-1316* later in this chapter.

1. Ensure that power to your VME system is off.

   The EPC-1316 module is not designed to be inserted or removed from "live" backplanes.

   When handling or inserting the EPC-1316 module, avoid touching the circuit board and connector pins, and ensure that the environment is static-free.

2. Ensure that the ejector handles are in the normal (non-eject) position. (Push the top handle down and the bottom handle up so that the handles are not tilted.)
3. Slide the EPC-1316 module into the slot. Use firm pressure on the handles to mate the module with the connectors.
4. Tighten the retaining screws in the top and bottom of the front panel to ensure proper connector mating and to prevent the module from loosening due to vibration.
5. Connect peripherals to the EPC-1316. Peripherals typically include a video display and keyboard, but also perhaps a mouse, modem, printer, and so on. For information about front-panel connector pinouts, see *Appendix C, Connectors*.

   Observe the following while the system is powered up:

   - Do not plug cables or connectors into the front panel connectors. Because electronics equipment generally cannot withstand fluctuations in power, damage can arise from plugging in a device or board while power is on.
   - Do not plug in a serial or parallel device, keyboard, transceiver, monitor or other component. This applies to equipment at either end of an interface cable.

6. Complete remaining steps as required. Typical remaining steps include:
   - BIOS configuration (For information about setting up the BIOS configuration, see *Chapter 3, BIOS configuration*.)
   - Driver software installation
   - Application software installation

   Your system may be preconfigured by your supplier or you may be required to perform these tasks yourself.

Maintaining and upgrading the EPC-1316

Occasionally you will want to perform maintenance (such as replacing the battery) or upgrades (such as adding options) on the EPC-1316. When this occurs, you must extract the board from the VME chassis, repair or install the desired option, then re-install the board in the VME chassis.

If your EPC-1316 includes an option, you may need to disassemble the boards before upgrades or maintenance, then re-assemble the boards before re-inserting the EPC-1316 into the VME chassis. The following sections describe how.

Extracting the EPC-1316

Before performing certain maintenance operations such as replacing the battery or upgrading memory, you must remove the EPC-1316 from the VME chassis:

1. Make sure that power to your VME system is off.

   The EPC-1316 module is not designed to be inserted or removed from "live" backplanes.

   When handling or inserting the EPC-1316 module, avoid touching the circuit board and connector pins, and ensure that the environment is static-free.

2. Loosen the retaining screws in the top and bottom of the front panel to prepare for connector release.
3. Move the ejector handles to the eject position: push the top handle up and the bottom handle down so that the handles appear tilted.
4. Slide the EPC-1316 module out of its slot. Pull firmly on the handles to release the module from the connectors.
5. If your EPC-1316 includes an option, disassemble the board as described in *Dis-assembling the EPC-1316*.

Dis-assembling the EPC-1316

To separate an option board from the main board:

1. Remove the EPC-1316 in the VME chassis as described in *Extracting the EPC-1316.*
2. Remove the option as described below:
   - **MSIO Carrier Board**: see *Disconnecting the MSIO Carrier Board* in *Appendix F, MSIO Carrier Board*.
   - **MSF option board**: see *Disconnecting the MSF option board* in *Appendix G, MSF option board*.
   - **Flash disk module**: see *Disconnecting the Flash module* in *Appendix H, Flash disk module*.
   - **PMC modules**: see *Disconnecting the Flash module* in *Appendix I, PMC modules*.

Replacing the battery

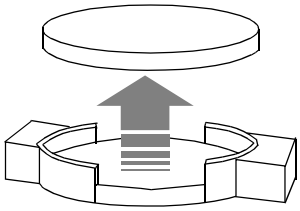
To replace the battery:

Perform these steps only in a static-free environment.

1. Before you begin, write down all the CMOS setup parameters while the battery is still good, or save them using the CMOS save and restore feature of the BIOS configuration *Exit menu* on page 46.
2. Turn off the power.

   If you leave the power on when removing the battery, setup values return to default conditions.

3. Remove the EPC-1316 from the VME chassis as described in *Extracting the EPC-1316*.
4. Locate the battery on the main board (see Figure C-1), then lift the battery out.



5. Press the new battery into place, positive (+) side up.

   There is danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by RadiSys. Dispose of used batteries according to manufacturer's instructions.

6. If your EPC-1316 includes an option, re-assemble the board as described in *Re-assembling the EPC-1316*.
7. Replace the EPC-1316 in the VME chassis as described in *Inserting the EPC-1316*.
8. Restore the CMOS settings as described in the *CMOS Save and Restore sub-menu* on page 48.

After removing the old battery, you can ship it to this address for disposal:

CPD Division Material Disposal
Program Management
c/o RadiSys Corporation
5445 NE Dawson Creek Drive
Hillsboro, OR USA 97124

Upgrading main system memory

Main memory is implemented as SODIMM 144-pin socketed 3.3 volts SDRAM. The main memory controller supports up to 256MB of PC100 SDRAM in two 144-pin SODIMM sockets.

It is best to populate the furthest SDRAM socket to reduce reflections. The first bank is labeled BANK1 on the silkscreen.

To add memory:

Perform these steps only in a static-free environment.

1. Obtain DRAM modules. At the time of writing, the following sizes of PC100 SDRAM were useable:

Type	Row/column	Total Size (MB)
4Mx64	12/10, 14/8	32
8Mx64	12/11, 14/9, 14/8	64
16Mx64	12/12, 14/10	128

Row and column numbers identify the DRAM configuration on the SODIMM modules.

2. Turn off the power.
3. Remove the EPC-1316 from the VME chassis as described in *Extracting the EPC-1316.*
4. If your EPC-1316 includes an option and it prevents you from accessing the SODIMM sockets, disassemble the board as described in *Dis-assembling the EPC-1316*.
5. Locate the SODIMM sockets on the Main board.
6. If your upgrade requires removal of existing DRAM modules:

   Avoid using excessive force as the SODIMM sockets are fragile.

   A. Gently push the socket's arms outward and tilt the module upward to clear the arm tabs.

   B. Pull slowly and parallel to the board to extract the DRAM from the socket.

   C. Repeat steps A and B for each module you need to remove.

7. Add DRAM modules:

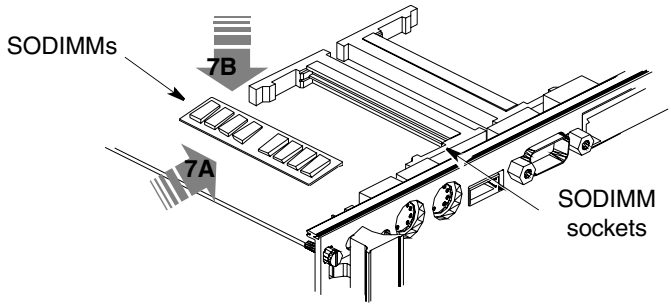


Figure 2-6. Inserting SODIMMs

A. Insert the DRAM module by sliding the edge fingers into the socket at almost a horizontal level, ensure that the module is fully home.

B. Apply a small pressure vertically onto the module while gently pushing the socket's arms outward. The module clicks into place when in the correct position.

8. If your EPC-1316 includes an option, re-assemble the board as described in *Re-assembling the EPC-1316*.
9. Replace the EPC-1316 in the VME chassis as described in *Inserting the EPC-1316*.

Installing other options

For information about installing other options available for the EPC-1316, see the appropriate appendix:

- **Flash disk module**: see *Appendix H, Flash disk module*.
- **PMC modules**: see *Appendix I, PMC modules*.

Re-assembling the EPC-1316

After performing maintenance operations such as replacing the battery or upgrading memory, you must re-connect the main board and option boards, and then re-install the EPC-1316 into the VME chassis.

To re-assemble the EPC-1316:

1. Install the option as described below:
   - **MSIO Carrier Board**: see *Re-assembling the MSIO Carrier Board and the Main board* in *Appendix F, MSIO Carrier Board*.
   - **MSF option board**: see *Re-assembling the MSF option board and the Main board* in *Appendix G, MSF option board*.
   - **Flash disk module**: see *Installing the Flash module* in *Appendix H, Flash disk module*.
   - **PMC modules**: see *Installing a PMC module on the Main board* in *Appendix I, PMC modules*.
2. Replace the EPC-1316 in the VME chassis as described in *Inserting the EPC-1316*.

3 BIOS configuration

The EPC-1316 uses the PhoenixBIOS to configure and select various system options. This chapter details the various menus and sub-menus used to configure the system.

This chapter is written as though you are setting up each field in sequence and for the first time. Your system may be correctly pre-configured and require very little setup.

You may see some error messages during the execution of the BIOS initialization sequence. If errors occur during the power-on self-test (POST), the BIOS displays the error on the appropriate line of the screen display and, depending on how your system is configured, either pauses or attempts to continue. For information about error messages, see *Appendix E, Error messages and diagnosis*.

BIOS setup screens

The EPC-1316's BIOS includes a setup program that displays and modifies the system configuration. This information is maintained in the EPC-1316's nonvolatile CMOS RAM and is used by the BIOS to initialize the EPC-1316 hardware.

You can enter the BIOS Setup only during the system reset process, following a power-up, front panel reset, or equivalent. To enter Setup, press the F2 key when prompted.

To revert to the original BIOS settings, do one of the following:

- Select Get Default Values from the *Exit menu* on page 46.
- Press the F9 key.

Select from the menus shown in the next table to set up the BIOS.

Table 3-1. BIOS Setup menu map

Menu	Sub-Menu
Main menu	Primary/Secondary Master/Slave sub-menus Keyboard Features sub-menu UBE Shadow Control sub-menu
Advanced Menu	PCI Configuration sub-menu I/O Device Configuration sub-menu Cache Memory sub-menu Advanced Chipset Control sub-menu
Security menu	None
Power menu	None
Boot menu	None
VME menu	None
Exit menu	CMOS Save and Restore sub-menu

Press the up and down cursor (arrow) keys to move from field to field. Press the right and left arrow keys to move between the menus as shown in the menu bar at the top of the screen. If you use the arrow keys to leave a menu and then return, your active field is always at the beginning of the menu. If you select a sub-menu and then return to the main menu, you return to that sub-menu heading.

Fields with a triangle to the left are actually sub-menu headings; press the Enter key when the cursor rests on one of these headings to reach that sub-menu. For most fields, position the cursor at the field and from the numeric keypad, press the + and – keys to rotate through the available choices. You can also use the Enter key to display choices. Certain numeric fields can also be entered via the keyboard. Once the entry has been changed to appear as desired, use the up and down arrow to move to the next field.

Additional help information is available in the help area on the Setup screen for each menu.

Main menu

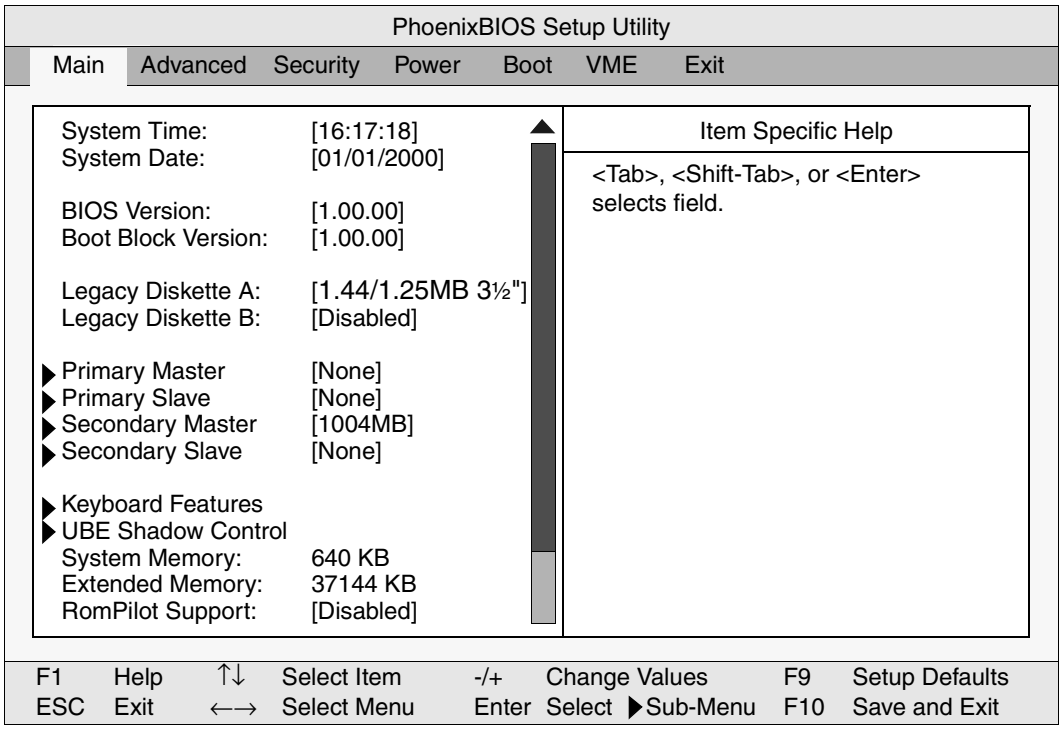


Figure 3-1. Main menu

The far right menu in the menu bar is the Exit Menu. Use the options in the Exit menu to save your changes, re-load default BIOS settings, and so on. Press the ESC key to go immediately to the Exit Menu.

The fields in each menu and sub-menu are explained below. Additional help information is available in the help area on the right side of each screen.

Field	Description
System Time/System Date	Sets the system time and date. To change these values, go to each field and enter the desired value. Press the tab key to move from hour to minute to second, or from month to day to year. There is no default value.
BIOS Version	Displays the BIOS version.
Boot Block Version	Displays the boot block version.
Legacy Diskette A/ Legacy Diskette B	Identifies the type of floppy disk drive installed as the A or B drive. Possible settings include: • Disabled (default for drive B:) • 360 KB, 5¼" • 1.2MB, 5¼" • 720 KB, 3½" • 1.44/1.25MB 3½" (default for drive A:) • 2.88 MB, 3½"
Primary Master sub-menu	Displays a menu that you use to enter information for the master IDE drive connected to the primary IDE controller. Once you enter the information, the drive shows as selected on this menu. For more information, see *Primary/Secondary Master/Slave sub-menus* on page 21.
Primary Slave sub-menu	Displays a menu that you use to enter information for the slave IDE drive connected to the primary IDE controller. Once you enter the information, the drive shows as selected on this menu. For more information, see *Primary/Secondary Master/Slave sub-menus* on page 21.
Secondary Master sub-menu	Displays a menu that you use to enter information for the master IDE drive connected to the secondary IDE controller. Once you enter the information, the drive shows as selected on this menu. For more information, see *Primary/Secondary Master/Slave sub-menus* on page 21.
Secondary Slave sub-menu	Displays a menu that you use to enter information for the slave IDE drive connected to the secondary IDE controller. Once you enter the information, this menu shows the drive selected. For more information, see *Primary/Secondary Master/Slave sub-menus* on page 21.
Keyboard Features sub-menu	Displays a menu that you can use to set and change the keyboard settings.
UBE Shadow Control sub-menu	Displays a menu that you use to control copying information from ROM into RAM and accessing it in the shadow (alternate) memory location. For more information, see *UBE Shadow Control sub-menu* on page 26.

Field	Description
System memory	Displays the amount of conventional memory (below 1MB). This field is not editable; no user interaction is required.
Extended memory	Displays the amount of extended memory (above 1MB). This field is not editable; no user interaction is required.
RomPilot† Support	Determines whether this system can access and use RomPilot software. RomPilot software manages an EPC-1316 system from a remote location. For detailed information, see *Appendix J, Installing and configuring RomPilot*. You can choose one of these: • **Disabled (default)**: You can manage this system only from this system. • **Enabled**: You can manage this system from a remote location, provided RomPilot is properly installed and configured.

Primary/Secondary Master/Slave sub-menus

There are a total of four IDE adapter sub-menus for the primary and secondary hard disk controllers, each having a master and slave drive menu.

Access this screen to:

- See or reconfigure the detailed characteristics of the primary hard disk (select the IDE Adapter 0 Master item from the Main BIOS Setup).
- Set up new disks and allow the Setup program to determine the proper settings based on information on the disk. Note that the Setup program can detect these settings only on drives that comply with ANSI specifications.
- Set up existing (formatted) disks. Note that you must use the same parameters used when the disk originally was formatted. You must select an option for the Type field, then enter the specific cylinder, head, and sector information listed on the label attached to the drive at the factory.

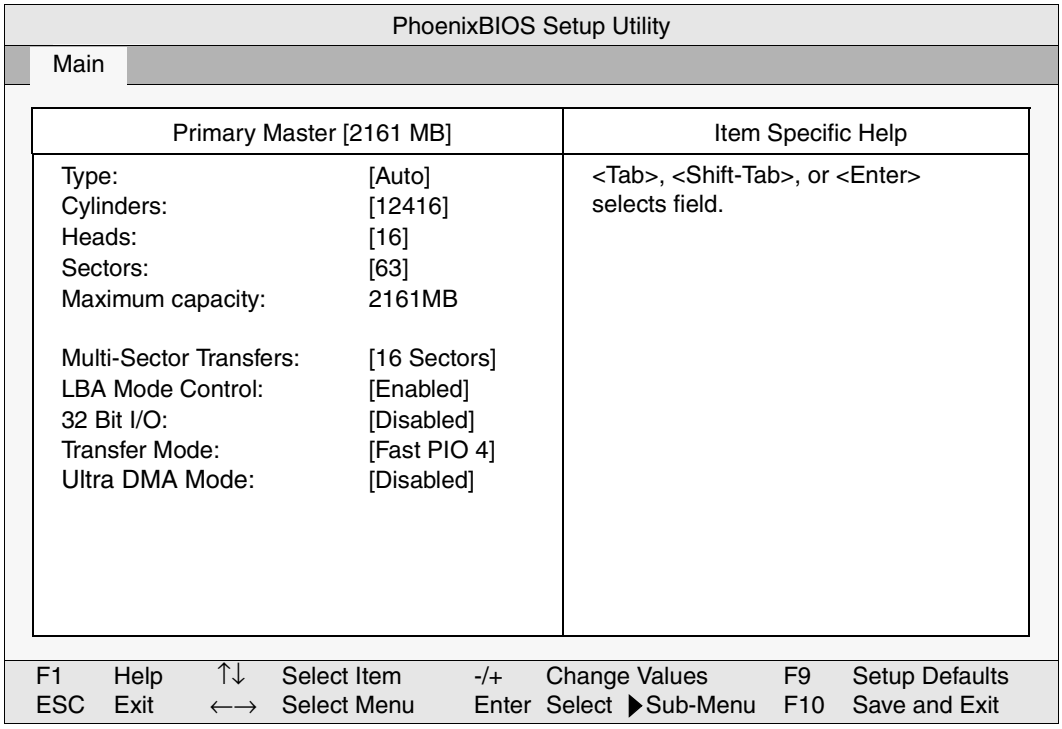

PhoenixBIOS Setup Utility
Main
Primary Master [2161 MB]
Item Specific Help
Type: [Auto]
Cylinders: [12416]
Heads: [16]
Sectors: [63]
Maximum capacity: 2161MB
Multi-Sector Transfers: [16 Sectors]
LBA Mode Control: [Enabled]
32 Bit I/O: [Disabled]
Transfer Mode: [Fast PIO 4]
Ultra DMA Mode: [Disabled]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-2. Master/Slave sub-menu

Field	Description
Type	Identifies the disk type.You can select one of these: • **Auto (default)**: Select this option when you want the POST to query the hard disk for its parameters whenever the POST runs. If a hard disk type is set to "Auto", but no hard disk is actually present, the BIOS queries the (non-existent) hard disk until it times out, adding a number of seconds to the duration of the POST. • **None**: Select this option if this adapter does not have an IDE hard disk drive. • **CD-ROM**: Select this option if this adapter has a CD-ROM drive. • **IDE Removable:** Provides support for high-capacity disks that can be formatted as floppy or hard disks. This option may be used for compact flash cards. • **ATAPI Removable**: Select this option if this adapter has a removable disk drive. • **Other ATAPI**: Select this option if the adapter has an ATAPI device that is not a CD-ROM or hard drive. • **User**: Select this option if you have an IDE disk but cannot use the "Autotype" feature. Then enter the correct drive values for cylinders, heads, sectors/track, and write precompensation. **Note**: For disks not supplied, consult the product's documentation. Once you complete setup for the IDE Master, you can choose the IDE Adapter 0 Slave sub-menu to configure your second drive. When finished, press the ESC key to return to the Main menu.
Cylinders	Displays the number of cylinders on this system. This field is only editable when you select User in the Type field.
Heads	Displays the number of heads on this system. This field is only editable when you select User in the Type field.
Sectors	Displays the number of sectors on this system. This field is only editable when you select User in the Type field.
Maximum Capacity	Displays the amount of disk space available on this system. This field is only editable when you select User in the Type field.

Field	Description
Multi-Sector Transfers	Allows the System BIOS to read ahead by the specified number of sectors whenever a disk access is performed. This has the effect of reading more data at once to reduce the absolute number of discrete disk reads performed by the operating system, which may increase system performance. You can select one of these: • Disabled (default if no drive is installed) • 2 sectors • 4 sectors • 8 sectors • 16 sectors (default if a drive is installed) Note that autotyping may change this value if the hard disk reports that it supports block accesses.
LBA Mode Control	Determines how the System BIOS references hard disk data. You can use this option only if both the hard disk being configured and the operating system support Logical Block Addressing (LBA). Autotyping may change this value if the hard disk reports that it supports LBA. You can select one of these: • **Disabled (default if no drive is installed)**: Reference hard disk data using the Cylinders/Heads/Sectors (CHS) method. • **Enabled (default if a drive is installed)**: Reference hard disk data as logical blocks.
32-bit I/O	Determines how the System BIOS accesses the hard disk controller. Autotyping does not affect this option. Accesses with 32-bit I/O accesses. This option increases system performance. • **Disabled (default)**: Select this option if an ISAbus IDE controller is installed in the system. • **Enabled**: Select this option to maximize system performance when the onboard PCI IDE controller is used.

Field	Description
Transfer Mode	Selects the mode that the System BIOS uses to access the hard disk. The selections include: • Standard (default if no drive is installed) • Fast PIO • Fast PIO 2 • Fast PIO 3 • Fast PIO 4 (default if a drive is installed) • FPIO4/DMA 2 • FPIO3/DMA 1 Older hard disks only support "Standard". Newer hard disks adhering to "Fast ATA" or "Enhanced IDE" specifications may support the fast programmed I/O or DMA modes. Note that autotyping may change this value depending on the transfer modes that the hard disk reports it supports. The fast DMA modes take full advantage of the onboard bus mastering hard disk controller and should yield the highest performance when used in conjunction with multitasking operating systems that support it.
Ultra DMA Mode	Selects the Ultra DMA mode used to copy data to and from the hard drive. Autotyping the drive automatically selects the optimum transfer mode. You can select one of these: • Disabled (default if no drive is installed) • Mode 0 • Mode 1 • Mode 2 (default if a drive is installed)

Keyboard Features sub-menu

The Keyboard Features sub-menu allows the user to set and change keyboard settings.

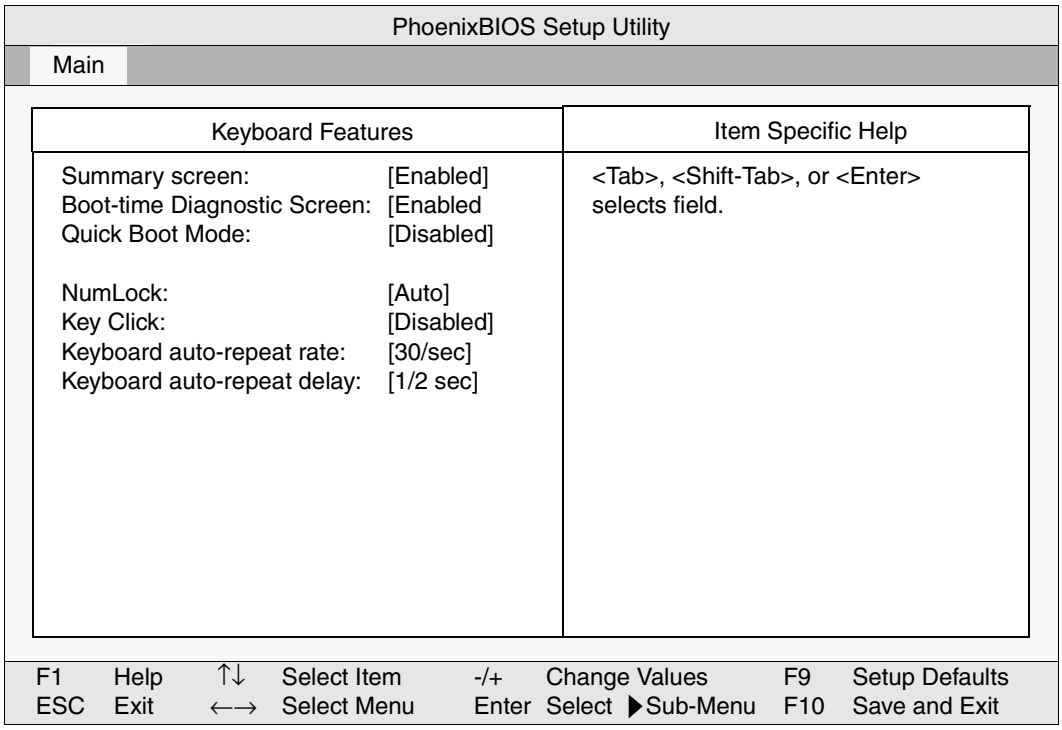

PhoenixBIOS Setup Utility
Main
Keyboard Features
Item Specific Help
Summary screen: [Enabled]
Boot-time Diagnostic Screen: [Enabled
Quick Boot Mode: [Disabled]
NumLock: [Auto]
Key Click: [Disabled]
Keyboard auto-repeat rate: [30/sec]
Keyboard auto-repeat delay: [1/2 sec]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-3. Keyboard Features sub-menu

Field	Description
Summary Screen	Determines whether the system configuration displays prior to loading the operating system. You can select one of these: • **Enabled (default)**: Displays a summary of the system configuration before the operating system starts to load • **Disabled**: Does not display a summary of the system configuration before the operating system starts to load. Selecting this option speeds up the boot process.
Boot-time Diagnostic Screen	Determines whether the system displays an OEM bitmap or the customary boot time diagnostic screen. You select one of these: • **Enabled (default)**: Displays an OEM bitmap. • **Disabled**: Displays the customary boot time diagnostic screen.
QuickBoot Mode	Determines whether the system runs selected tests during boot-up. You can select one of these: • **Disabled (default)**: Runs tests during boot. • **Enabled**: Does not run tests during boot. Selecting this option speeds up the boot process.

Field	Description
NumLock	Determines whether the keyboard numbers (the NumLock feature) operates. You can select one of these: • **Auto (default)**: • **Off**: Disengages the NumLock key at boot. • **On**: Engages the NumLock key at boot.
Key Click	Determines whether the keyboard produces an audible click each time a key is pressed. You can select one of these: • **Disabled (default)**: The keyboard does not produce audible clicks when keys are pressed. • **Enabled**: The keyboard produces an audible click each time a key is pressed.
Keyboard Auto-repeat Rate	Determines the number of keystrokes entered per second holding a key down on the keyboard. You can select one of these: • 30/sec (default) • 26.7/sec • 21.8/sec • 18.5/sec • 13.3/sec • 10/sec • 6/sec • 2/sec
Keyboard Auto-repeat Delay	Sets the delay between when a key is pressed and when the auto-repeat feature begins. You can select one of these: • ½ sec (default) • ¼ sec • ¾ sec • 1 sec

UBE Shadow Control sub-menu

Shadowing refers to the technique of copying BIOS extensions from ROM into DRAM and accessing them from DRAM. This allows the CPU to access the BIOS extensions much more quickly and generally increases system performance if many calls to the BIOS extensions are made.

About shadow memory regions

There is no effect on the system if a region is shadowed that does not contain a BIOS extension. Note that each shadow region in the setup menu is 16KB in size. Multiple shadow regions may have to be enabled if the BIOS extension to be shadowed is larger than 16KB.

For example, if you select a source offset of 18000h, a destination of D4000h, and a size of 16KB, the BIOS will shadow the contents of 98000h–A0000h in the FBD (as measured from the base of the FBD) to D4000h–DC000h in memory.

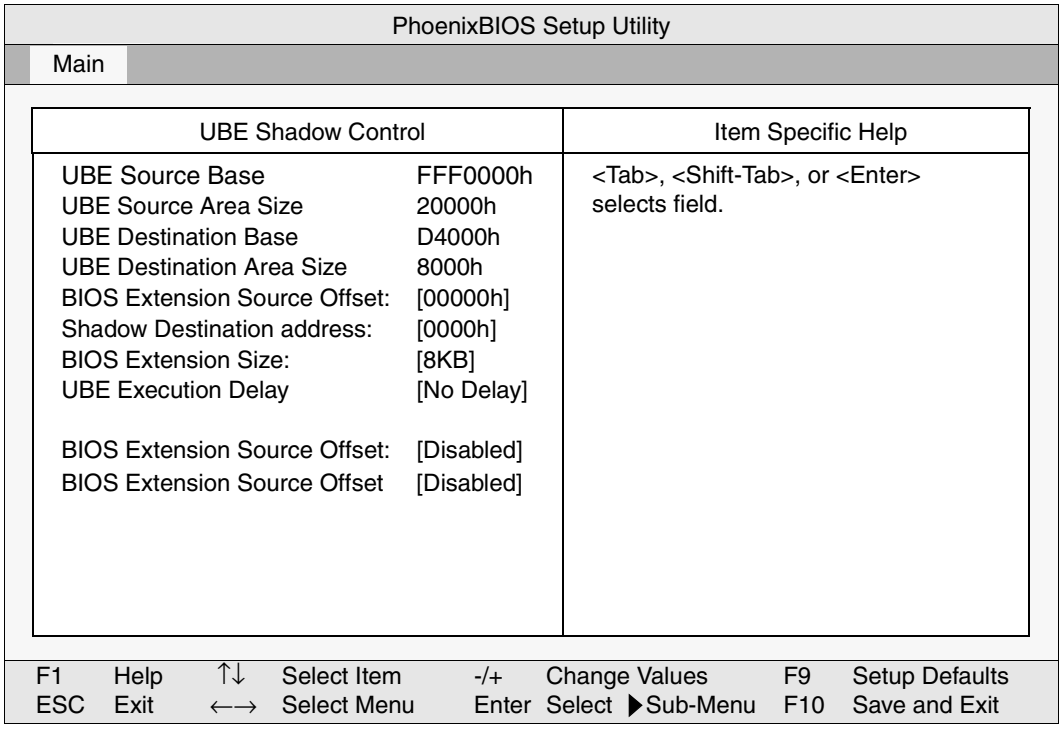

PhoenixBIOS Setup Utility
Main
UBE Shadow Control
Item Specific Help
UBE Source Base FFF0000h
UBE Source Area Size 20000h
UBE Destination Base D4000h
UBE Destination Area Size 8000h
BIOS Extension Source Offset: [00000h]
Shadow Destination address: [0000h]
BIOS Extension Size: [8KB]
UBE Execution Delay [No Delay]
BIOS Extension Source Offset: [Disabled]
BIOS Extension Source Offset [Disabled]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-4. UBE Shadow Control sub-menu

Field	Description
BIOS Extension Source Offset	Specifies the location of the BIOS extension from the base address of main block #5 of the Flash Boot Device. You can select one of these: • Disabled (default) • 0000h • 2000h • 4000h • 6000h • 8000h • A000h • C000h • E000h • 10000h • 12000h • 14000h • 16000h • 18000h • 1A000h • 1C000h
Shadow Destination Address	Specifies the destination offset from the UBE “Destination Base” address. You can select one of these: • 0000h (default) • 2000h • 4000h • 6000h • **Note**: This field displays only if the BIOS Extension Source field contains a value other than [Disabled].

Field	Description
BIOS Extension Size	Specifies, in bytes, the BIOS extension's size. You can select one of these: • 8KB (default) • 16KB • 24KB • 32KB **Note**: This field displays only if the BIOS Extension Source field contains a value other than [Disabled].
UBE Execution Delay	Specifies the amount of execution delay. You can select one of these: • No delay (default) • 1 sec • 2 sec • 3 sec • 4 sec • 5 sec • 6 sec • 7 sec **Note**: This field displays only if the BIOS Extension Source field contains a value other than [Disabled].

Advanced Menu

This menu contains settings for integrated peripherals, memory shadow, cache, and large disk access mode. You access this menu by selecting Advanced from the Main BIOS Setup menu.

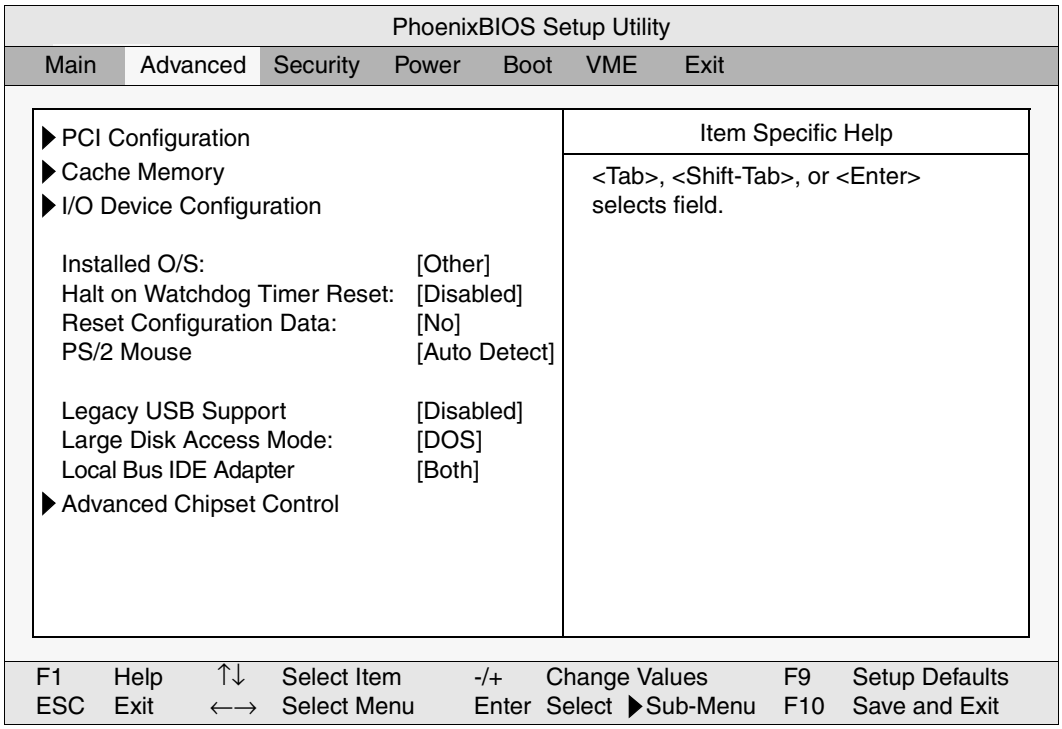


Figure 3-5. Advanced menu

Field	Description
PCI Configuration sub-menu	Displays a menu that you use to enter configuration information for PCI devices. For more information, see *PCI Configuration sub-menu* on page 31.
Cache Memory sub-menu	Displays a menu that you use to control the use of CPU cache. For more information, see *Cache Memory sub-menu* on page 34
I/O Device Configuration sub-menu	Displays a menu that you use to configure peripheral devices. For more information, see *I/O Device Configuration sub-menu* on page 37.
Installed OS	Identifies the OS you plan to use on this system. You can select one of these: • **Other (default)**: Select this option when you plan to use an OS other than Windows 95, Windows 98 or Windows 2000. • **Win95 OS**: Select this option when you plan to use a Windows 95 OS. **Note**: Setting this to the incorrect value may produce unexpected results.

Field	Description
Halt on Watchdog Timer Reset	Determines what happens when a watchdog timer reset occurs: • **Disabled (default)**: The boot process continues. • **Enabled**: The System BIOS halts the boot process.
Reset Configuration Data	Determines whether to clear the Extended System Configuration Data (ESCD) block that resides in the Flash Boot Device (FBD) parameter block #2. You can select one of these: • **No (default)**: Does not clear the ESCD block. • **Yes**: Clears the ESCD block. You must clear the block the first time a system is turned on or if the ESCD becomes corrupted. This option automatically resets to "No" after the block is cleared.
PS/2 Mouse	Determines whether a PS/2 mouse functions on this system. You can select one of these: • **Auto Detect (default)**: Allows the system BIOS to determine whether a PS/2 mouse functions on this system. • **Disabled**: Prevents any installed PS/2 mouse from functioning and frees IRQ 12. • **Enabled**: Sets the system to use a PS/2 mouse, if installed.
Legacy USB Support	Determines whether the system supports the Legacy Universal Serial Bus (USB). You can select one of these: • **Disabled (default)**: The system does not support the Legacy USB • **Enabled**: The system supports the Legacy USB.
Large Disk Access Mode	Specifies whether MS-DOS systems can use hard disks up to 8GB (1024C x 255H x 63S) without special drivers or LBA. If the drive fails while installing new software, change this setting and try again. You can select one of these: • **DOS (default)**: Causes the System BIOS to perform cylinder/head translation, if the drive is configured in Setup to have more than 1024 cylinders. Select this option if your system uses a drive larger than 528 MB and runs DOS or MS-DOS†. • **Other**: Select this option if your system uses a drive larger than 528 MB and runs an OS other than DOS or MS-DOS.
Local Bus IDE Adapter	Configures the integrated local bus IDE adapter. You can select one of these: • Primary (default) • Secondary • Both • Disabled
Advanced Chipset Control sub-menu	Displays a menu that you use to configure the PCI-chipset. For more information, see *Advanced Chipset Control sub-menu* on page 39

PCI Configuration sub-menu

Use the options in this sub-menu to control the exclusion of the UMB region for PCI or ISA and the exclusion of the IRQs for PCI or ISA

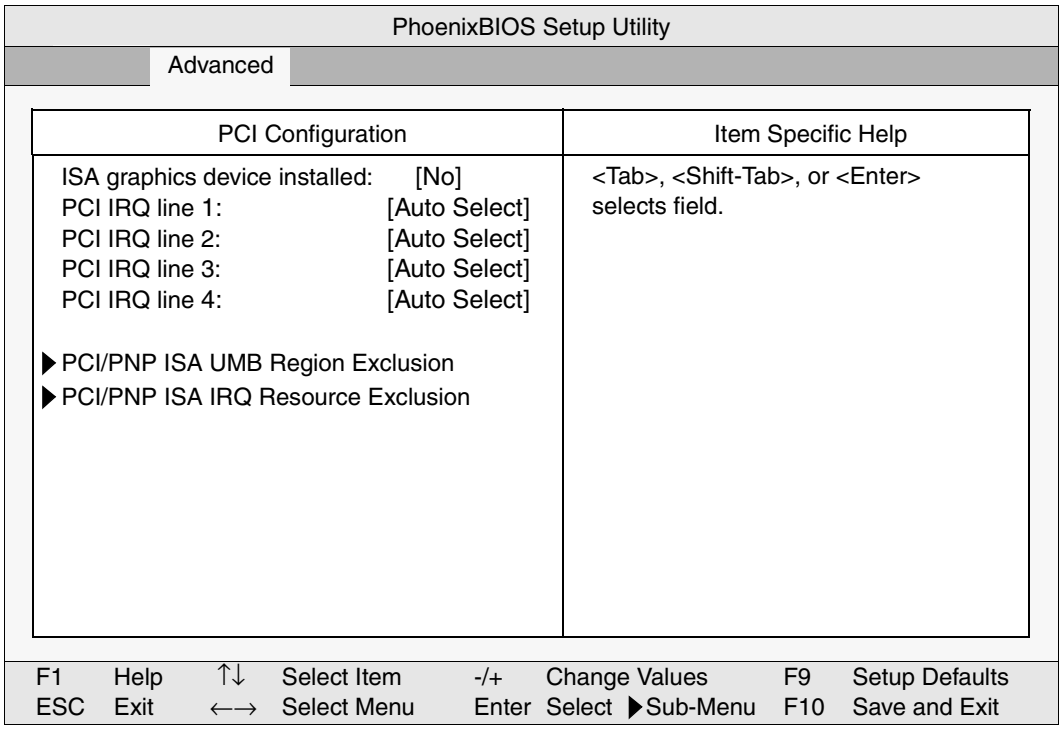

PhoenixBIOS Setup Utility
Advanced
PCI Configuration
Item Specific Help
ISA graphics device installed: [No]
PCI IRQ line 1: [Auto Select]
PCI IRQ line 2: [Auto Select]
PCI IRQ line 3: [Auto Select]
PCI IRQ line 4: [Auto Select]
PCI/PNP ISA UMB Region Exclusion
PCI/PNP ISA IRQ Resource Exclusion
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-6. PCI Configuration sub-menu

Field	Description
ISA graphics device installed	Specifies whether an ISA graphics device is installed in the system. • **No (default)**: No ISA graphics device exists in this system. • **Yes**: An ISA graphics device exists in this system.
PCI IRQ lines	Determines which IRQ the PCI IRQ (PIRQ) lines (1–4) use. You can select one of these: • Auto Select (default) • 3 • 4 • 5 • 7 • 9 • 11 • 12 • 14 • 15 • Disabled
PCI/PNP ISA UMB Region Exclusion sub-menu	Displays a menu that you use to control the exclusion of PCI and ISA UMB regions. For more information, see *PCI/PNP ISA UMB Region Exclusion sub-menu* on page 32.
PCI/PNP ISA IRQ Resource Exclusion sub-menu	Displays a menu that you use to control the exclusion of PCI and ISA interrupt resources. For more information, see PCI/PNP ISA IRQ Resource Exclusion sub-menu on page 33.

PCI/PNP ISA UMB Region Exclusion sub-menu

The PCI/PNP ISA UMB Region Exclusion sub-menu control the exclusion of PCI and ISA UMB regions.

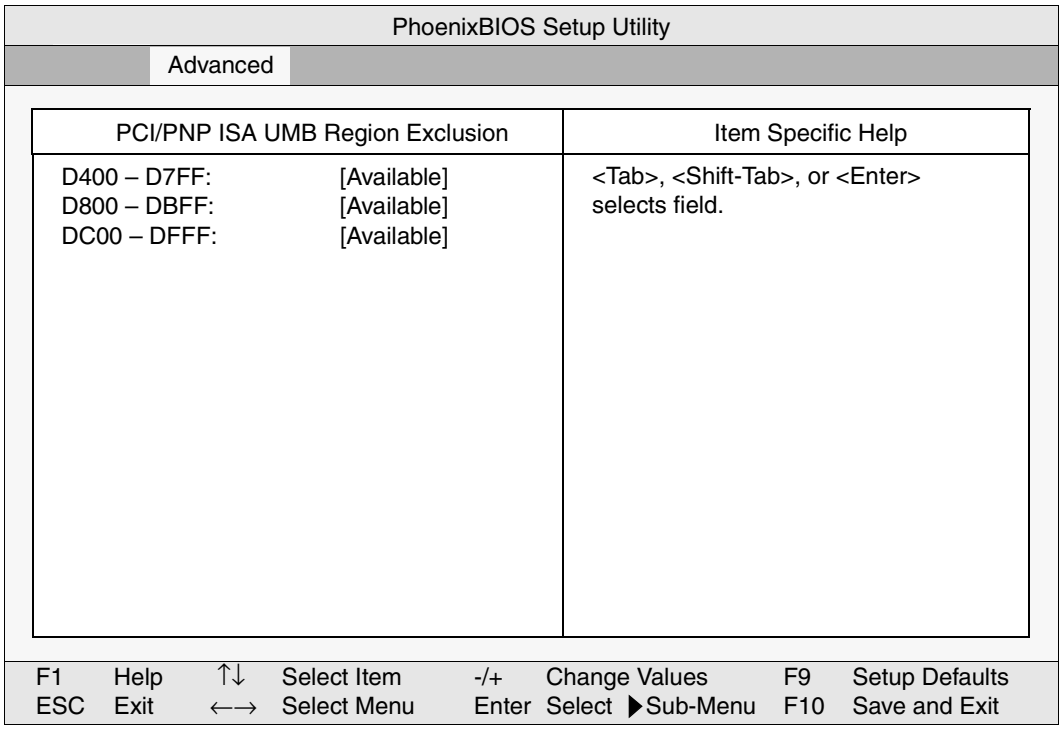

PhoenixBIOS Setup Utility
Advanced
PCI/PNP ISA UMB Region Exclusion
Item Specific Help
D400 – D7FF: [Available]
D800 – DBFF: [Available]
DC00 – DFFF: [Available]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-7. PCI/PNP ISA UMB Region Exclusion sub-menu

Field	Description
Memory Regions	Determines the use of each UMB region. You can select one of these: • **Available (default)**: Makes the regions available for PCI use. • **Reserved**: Reserves the specified block of upper memory regions for ISA use.

PCI/PNP ISA IRQ Resource Exclusion sub-menu

The PCI/PNP ISA IRQ Resource Exclusion Sub-Menu controls the exclusion of PCI and ISA interrupt regions.

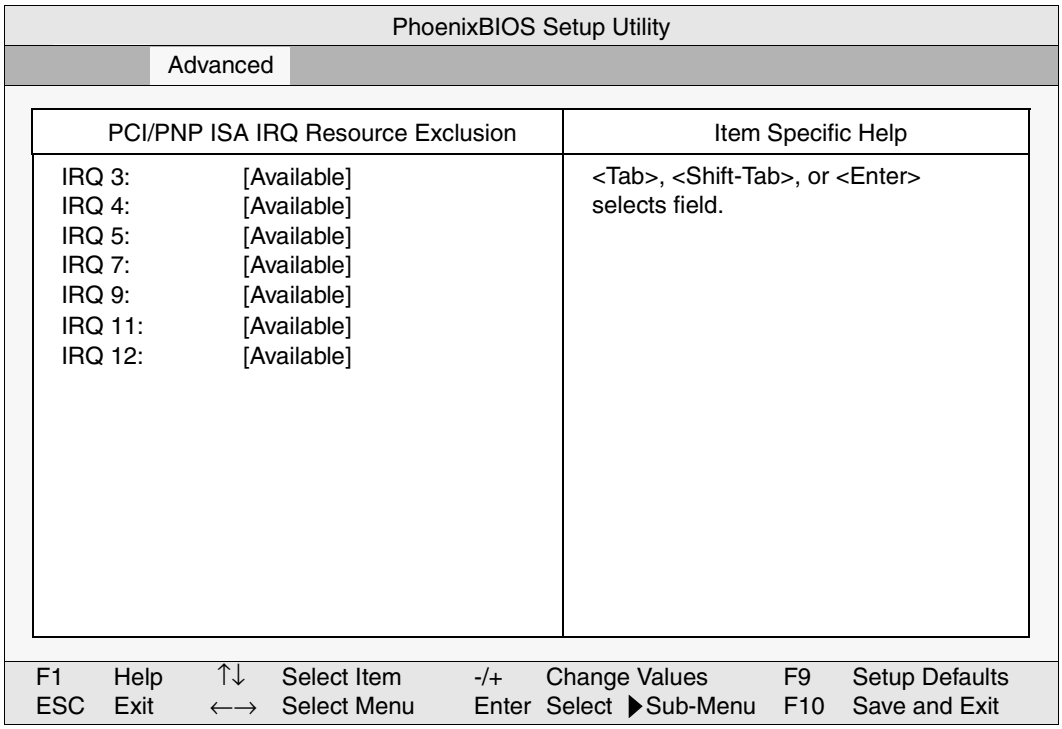

PhoenixBIOS Setup Utility
Advanced
PCI/PNP ISA IRQ Resource Exclusion
Item Specific Help
IRQ 3: [Available]
IRQ 4: [Available]
IRQ 5: [Available]
IRQ 7: [Available]
IRQ 9: [Available]
IRQ 11: [Available]
IRQ 12: [Available]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-8. PCI/PNP ISA IRQ Resource Exclusion sub-menu

Field	Description
Interrupts	Determines the use of each interrupt. You can select one of these: • **Available (default)**: Makes the specified ISA IRQs available for PCI use. • **Reserved**: Reserves the interrupt for ISA use.

Cache Memory sub-menu

The options in this screen control the cacheability of certain memory regions and also the settings of the Level 2 (L2) cache.

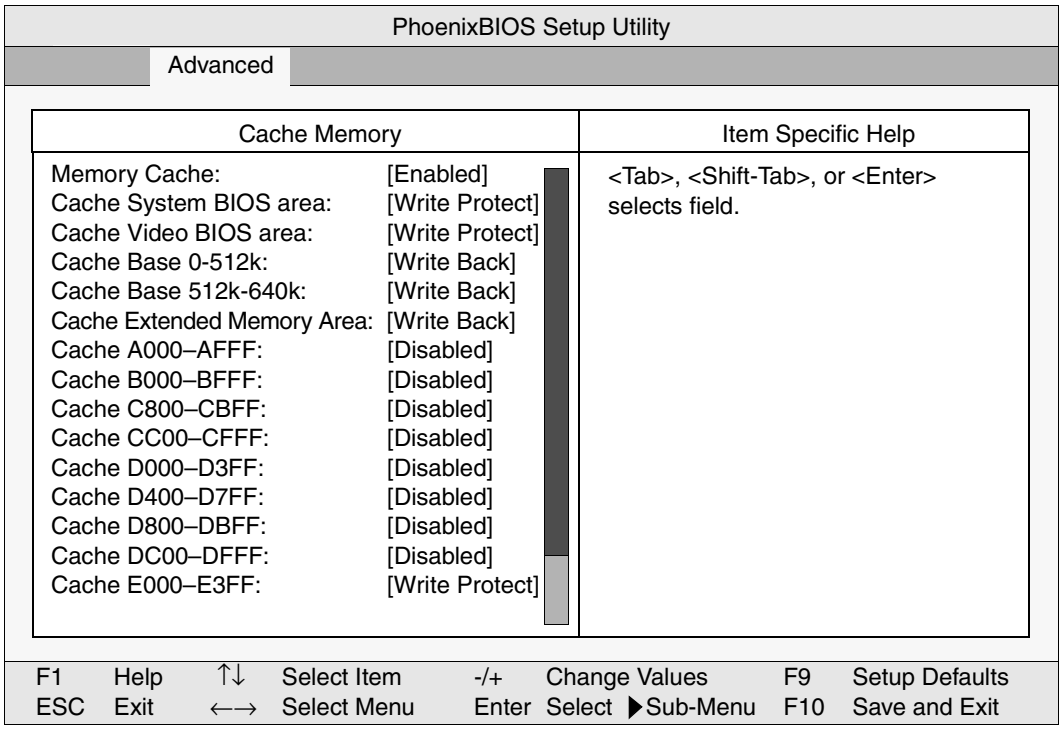

PhoenixBIOS Setup Utility
Advanced
Cache Memory
Item Specific Help
Memory Cache: [Enabled]
Cache System BIOS area: [Write Protect]
Cache Video BIOS area: [Write Protect]
Cache Base 0-512k: [Write Back]
Cache Base 512k-640k: [Write Back]
Cache Extended Memory Area: [Write Back]
Cache A000–AFFF: [Disabled]
Cache B000–BFFF: [Disabled]
Cache C800–CBFF: [Disabled]
Cache CC00–CFFF: [Disabled]
Cache D000–D3FF: [Disabled]
Cache D400–D7FF: [Disabled]
Cache D800–DBFF: [Disabled]
Cache DC00–DFFF: [Disabled]
Cache E000–E3FF: [Write Protect]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-9. Cache memory sub-menu

Field	Description
Memory Cache	Enables (default) or disables memory caching.
Cache System BIOS Area	Determines whether the System BIOS is cached in DRAM. You can select one of these: • **Write Protect (default)**: caches the System BIOS in the 0E0000h through 0FFFFFh DRAM area. • **uncached**: Does not cache the system BIOS.
Cache Video BIOS Area	Determines whether the VGA BIOS is cached in a region. You can select one of these: • **Write Protect (default)**: caches the VGA BIOS in the 0C0000h through 0C7FFFh region. • **uncached**: Does not cache the VGA BIOS.

Field	Description
Cache Bases	Determines how the system caches base memory. You can select one of these: • **Write Back (default)**: Writes and reads to and from system memory are cached, then written to system memory when you perform a write-back operation. Select this option to reduce bus traffic by eliminating unnecessary writes to system memory. This option provides the best performance, but requires that all devices that access system memory on the system bus be able to snoop memory accesses to ensure system memory and cache coherency. • **Write Through**: Writes and reads to and from system memory are cached. Select this option for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. • **Write Protect**: Reads come from cache lines when possible, and read misses cause cache fills. Writes are propagated to the system bus and cause corresponding cache lines on all processors on the bus to be invalidated. Speculative reads are allowed. • **uncached**: The system does not cache memory.
Cache Extended Memory Area	Determines how the system caches extended memory. You can select one of these: • **Write Back (default)**: Writes and reads to and from system memory are cached, then written to system memory when you perform a write-back operation. Select this option to reduce bus traffic by eliminating unnecessary writes to system memory. This option provides the best performance, but requires that all devices that access system memory on the system bus be able to snoop memory accesses to ensure system memory and cache coherency. • **Write Through**: Writes and reads to and from system memory are cached. Select this option for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. • **Write Protect**: Reads come from cache lines when possible, and read misses cause cache fills. Writes are propagated to the system bus and cause corresponding cache lines on all processors on the bus to be invalidated. Speculative reads are allowed. • **uncached**: The system does not cache memory.

Field	Description
Cache Memory Regions	Determines how the system deals with specified memory blocks or shadow[1] memory. You can select one of these: • **Disabled (default)**: The system does not cache memory. • **USWC Caching**: System memory locations are not cached (as with uncacheable memory) and coherency is not enforced by the processor's bus coherency protocol. Speculative reads are allowed. Writes may be delayed and combined in the write buffer to reduce memory accesses. Select this option for video frame buffers, where the order of writes is unimportant as long as the writes update memory so they can be seen on the graphics display. • **Write Through**: Writes and reads to and from system memory are cached. Select this option for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. • **Write Protect**: Reads come from cache lines when possible, and read misses cause cache fills. Writes propagate to the system bus and cause corresponding cache lines on all processors on the bus to be invalidated. Speculative reads are allowed. • **Write Back**: Writes and reads to and from system memory are cached, then written to system memory when you perform a write-back operation. Select this option to reduce bus traffic by eliminating unnecessary writes to system memory. This option provides the best performance, but requires that all devices that access system memory on the system bus be able to snoop memory accesses to ensure system memory and cache coherency. When BIOS extensions are present in these regions, enabling caching for that region increases performance.

I/O Device Configuration sub-menu

Use the options in this sub-menu to configure the onboard serial and parallel port and disk controllers.

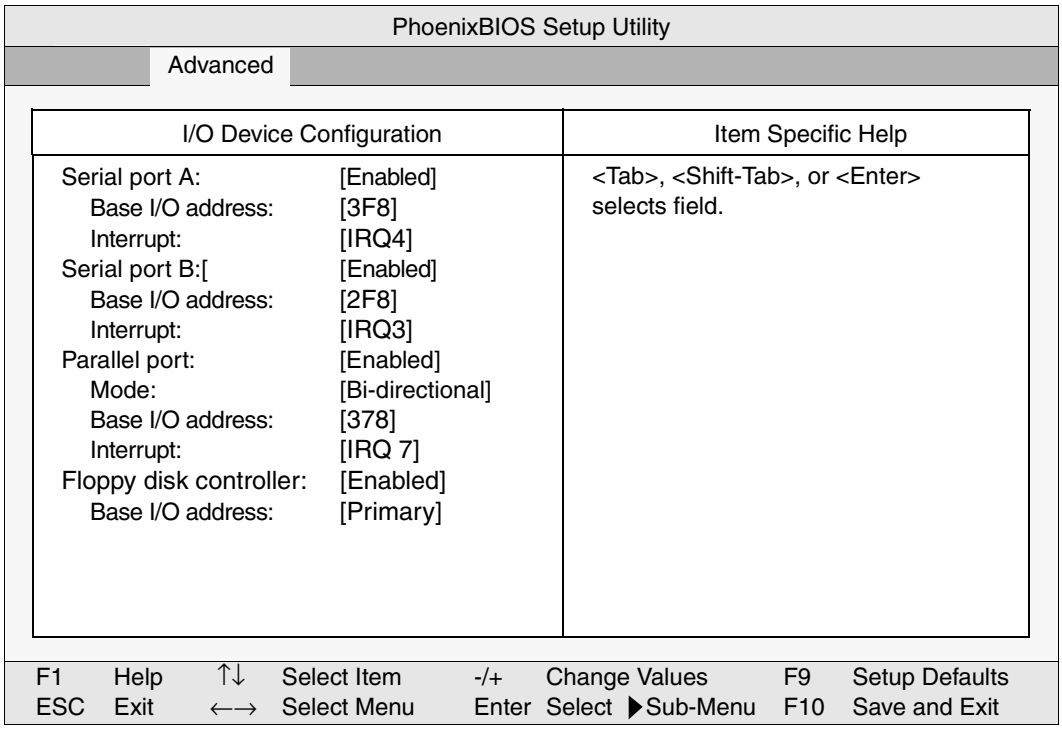

PhoenixBIOS Setup Utility
Advanced
I/O Device Configuration
Item Specific Help
Serial port A: [Enabled]
Base I/O address: [3F8]
Interrupt: [IRQ4]
Serial port B:[[Enabled]
Base I/O address: [2F8]
Interrupt: [IRQ3]
Parallel port: [Enabled]
Mode: [Bi-directional]
Base I/O address: [378]
Interrupt: [IRQ 7]
Floppy disk controller: [Enabled]
Base I/O address: [Primary]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-10. I/O Device Configuration sub-menu

Field	Description
Serial port A/Serial port B	Configures the selected serial port, labelled COM A or COM B. You can select one of these: • **Enabled (default)**: The serial port is configured. • **Auto**: Either the BIOS or OS configures the serial port. • **Disabled**: The serial port is not configured.
Base I/O Address	Configures the base address for the selected serial port. If you select a value already used by another serial port, an asterisk displays at the left side of the screen. You can select one of these: • 2F8/IRQ3 (default, Port B) • 3E8 • 3F8/IRQ4 (default, Port A) • 2E8 **Note**: This field displays only if the Serial Port field contains a value of [Enabled].

Field	Description
Interrupt	Configures the interrupt for the selected serial port. If you select a value already used by another serial port, an asterisk displays at the left side of the screen. You can select one of these: • IRQ3 (default, Port A) • IRQ4 (default, Port B) **Note**: This field displays only if the Serial Port field contains a value of [Enabled].
Parallel port	Configures the parallel port, labelled LPT. You can select one of these: • **Enabled (default)**: The parallel port is configured. • **Disabled**: The parallel port is not configured. • **Auto**: Either the BIOS or OS configures the parallel port.
Mode	Configures the mode for the parallel port. You can select one of these: • Bi-directional (default) • Output only • EPP • ECP **Note**: This field displays only if the Parallel Port field contains a value of [Enabled], [OS Controlled], or [Auto].
Base I/O address	Configures the I/O base address for the parallel port. You can select one of these: • 378 (default) • 278 • 3BC **Note**: This field displays only if the Parallel Port field contains a value of [Enabled].
Interrupt	Specifies which interrupt line the parallel port uses. You can select one of these: • IRQ7 (default) • IRQ5 **Note**: This field displays only if the Parallel Port field contains a value of [Enabled].
Floppy disk controller	Determines whether the floppy disk controller is available for use. You can select one of these: • **Enabled (default)**: User configuration. • **Disabled**: No configuration. • **Auto** Either the BIOS or OS configures the floppy disk controller.

Field	Description
Base I/O address	Configures the I/O base address for the floppy disk controller. You can select one of these: • Primary (default) • Secondary **Note**: This field displays only if the Parallel Port field contains a value of [Enabled].

Advanced Chipset Control sub-menu

Use the options in this sub-menu to configure the PCI chipset.

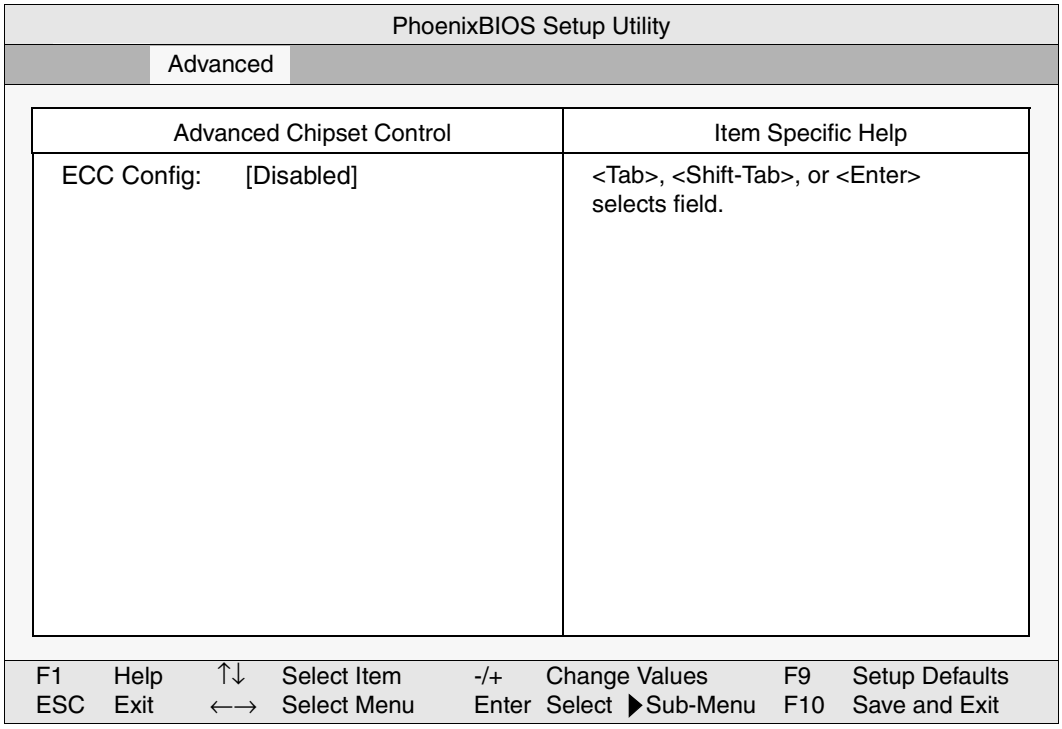

PhoenixBIOS Setup Utility
Advanced
Advanced Chipset Control
Item Specific Help
ECC Config: [Disabled]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-11. Advanced Chipset Control sub-menu

Field	Description
ECC Config	• Disabled (default) • EC • ECC • ECC Scrub

Security menu

The Security menu sets and changes passwords and security features. The supervisor password gives unrestricted access to vie and change all setup options. The user password restricts who can view and change setup options.

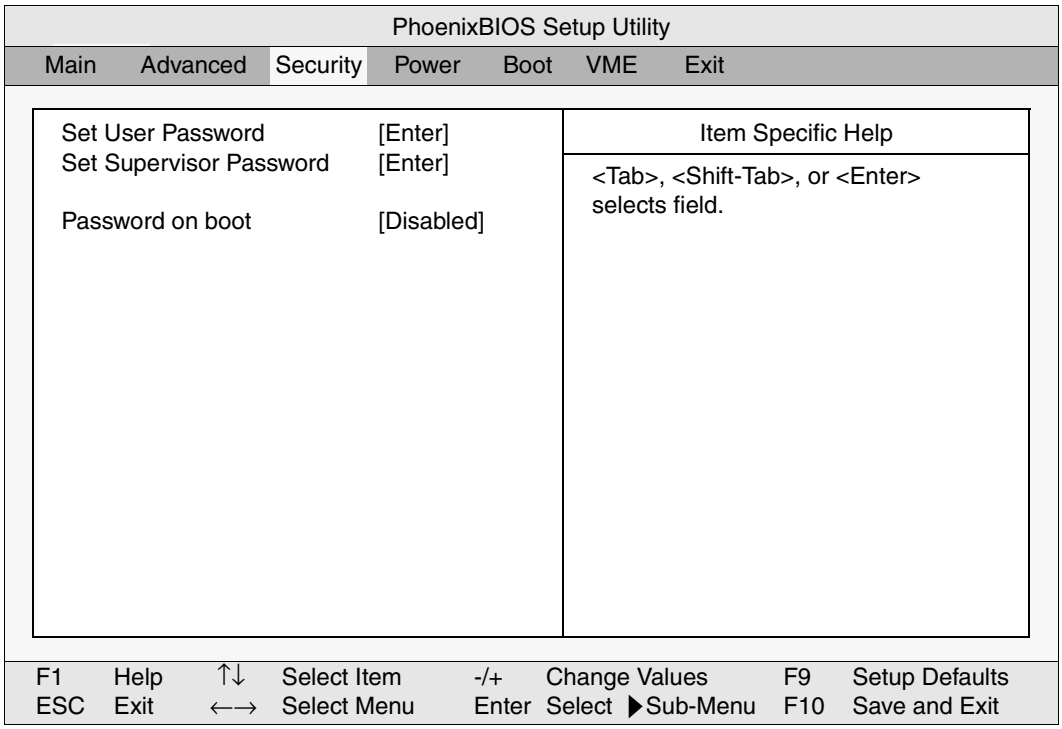

PhoenixBIOS Setup Utility
Main Advanced Security Power Boot VME Exit
Set User Password [Enter]
Set Supervisor Password [Enter]
Password on boot [Disabled]
Item Specific Help
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-12. Security menu

Field	Description
Set User Password	Sets the user password. When you select this field, the program prompts you to enter and confirm your password. Note: Before you can enter a value in this field, the supervisor password must contain a password.
Set Supervisor Password	Sets supervisor's password. When you select this field, the program prompts you to enter and confirm your password.
Password on Boot	Determines whether the user must enter a password before the system boots. You can select one of these: • **Disabled (default)**: Password is not required. • **Enabled**: Password is required.

Power menu

Options in this menu control power facilities.

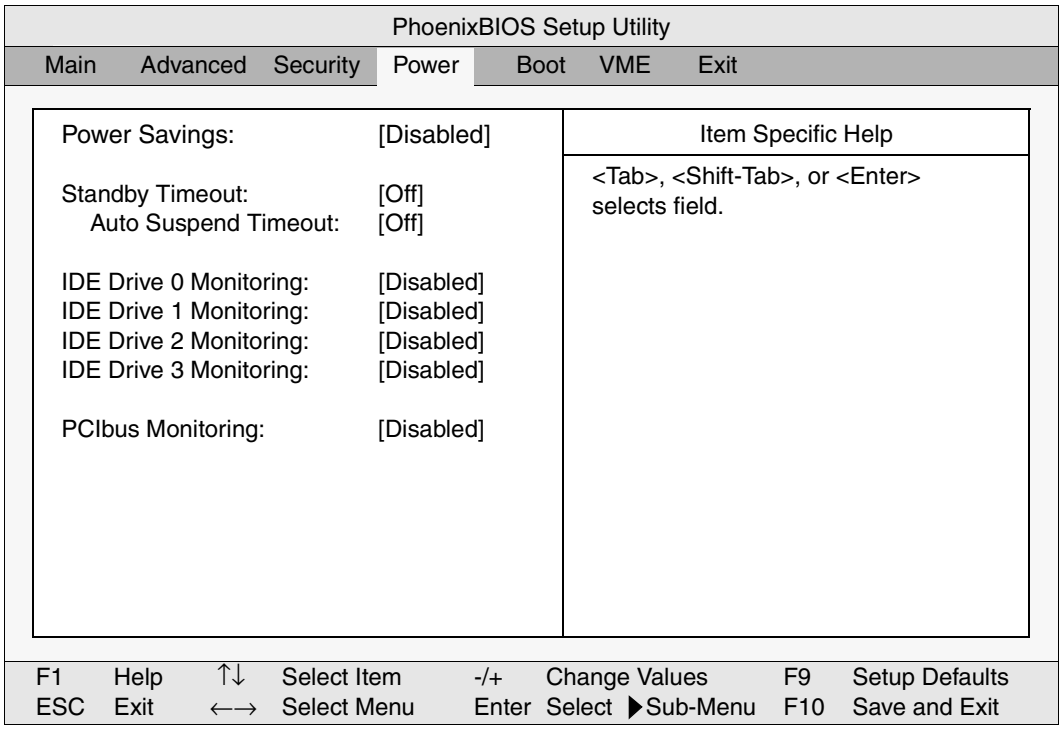

PhoenixBIOS Setup Utility
Main Advanced Security Power Boot VME Exit
Power Savings: [Disabled]
Standby Timeout: [Off]
Auto Suspend Timeout: [Off]
IDE Drive 0 Monitoring: [Disabled]
IDE Drive 1 Monitoring: [Disabled]
IDE Drive 2 Monitoring: [Disabled]
IDE Drive 3 Monitoring: [Disabled]
PCIbus Monitoring: [Disabled]
Item Specific Help
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-13. Power menu

Field	Description
Power Savings	Determines the type, if any, of power management. You can select one of these: • Disabled (default) • Customized • Maximum Power Savings • Maximum Performance
Standby Timeout	Determines the inactivity duration, if any, required to elapse before the system is placed in Standby Mode. You can select one of these: • Off (default) • 1 Minutes (default if Power Savings is set to Maximum Power Savings) • 2 Minutes • 4 Minutes • 6 Minutes • 8 Minutes • 12 Minutes • 16 Minutes (default if Power Savings is set to Maximum Performance) **Note**: You can edit this field only if Power Savings is set to Customized.

Field	Description
Auto Suspend Timeout	Sets the inactivity duration, if any, required to elapse before the system goes into Suspend Mode from Standby Mode. You can select one of these: • Off (default) • 5 Minutes (default if Power Savings is set to Maximum Battery Life) • 10 Minutes • 15 Minutes • 20 Minutes • 30 Minutes • 40 Minutes • 60 Minutes (default if Power Savings is set to Maximum Performance) **Note**: You can edit this field only if Power Savings is set to Customized.
IDE Drive 0–3 Monitoring	Determines whether activity is generated on the IDE device (required to keep the system awake). You can select one of these: • **Disabled (default)**: No activity occurs on the IDE device. • **Enabled**: Activity is generated on the IDE device.
PCIbus Monitoring	Determines whether activity is generated on the PCIbus (required to keep the system awake). You can select one of these: • **Disabled (default)**: No activity occurs on the PCIbus. • **Enabled**: Activity is generated on the PCIbus.

Boot menu

The Boot menu changes boot sequence options.

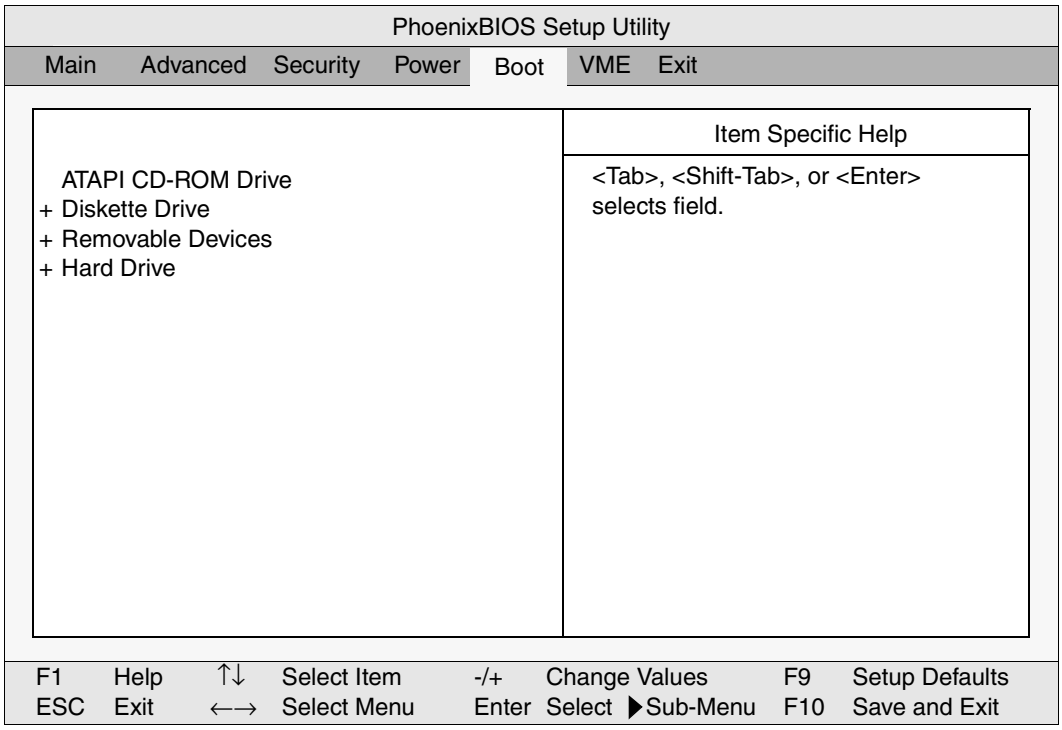

PhoenixBIOS Setup Utility
Main Advanced Security Power Boot VME Exit
Item Specific Help
<Tab>, <Shift-Tab>, or <Enter> selects field.
ATAPI CD-ROM Drive
+ Diskette Drive
+ Removable Devices
+ Hard Drive
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-14. Boot menu

To move an item to a higher level in the list, highlight the item and then press the "+" key. To move an item to a lower level in the list, highlight the item and then press the "–" key.

To display all boot device sub-menus under all respective device types, press the Ctrl and Enter keys at the same time.

To display a sub-menu that lists all devices of a specified type available on the system, highlight the device type and press the Enter key. If more than one device of that type exists, use the "+" and "–" keys to change the boot order within the given device type.

Field	Description
Boot order	Determines the boot order of boot devices. This is the default boot order: 1. ATAPI CD-ROM Drive 2. Diskette Drive 3. Removable Devices 4. Hard Drive

VME menu

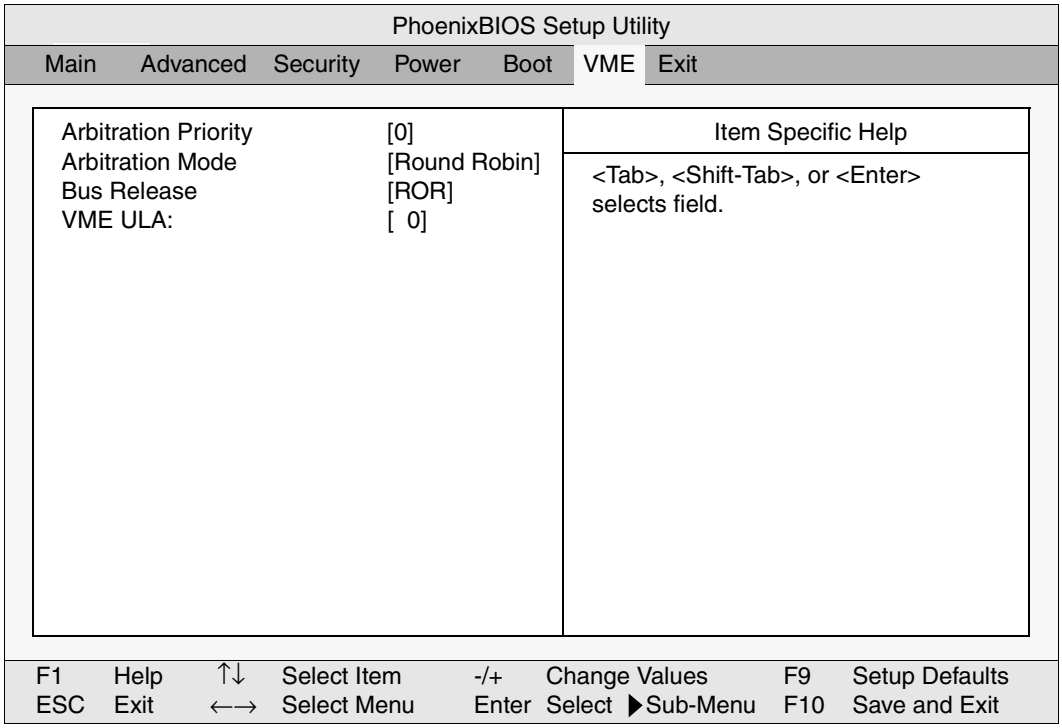

PhoenixBIOS Setup Utility
Main Advanced Security Power Boot VME Exit
Arbitration Priority [0]
Arbitration Mode [Round Robin]
Bus Release [ROR]
VME ULA: [0]
Item Specific Help
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-15. VME menu

Field	Description
Arbitration Priority	Selects the VMEbus priority levels used when the EPC-1316 requests the bus for a VME access: • 0 (default; lowest priority) • 1 • 2 • 3 (highest priority)
Arbitration Mode	Selects the arbitration algorithm that the EPC-1316's VMEbus arbiter uses when the EPC-1316 is the Slot 1 controller. You can select one of these: • **Round Robin (default)**: Configures the arbiter to "scan" the bus request lines from highest priority down to lowest priority and grant the bus to the first requester it finds. The four bus lines have equal priority. • **Priority**: Configures the arbiter to grant the bus to the highest priority requester at any time. Bus request 0 has the highest priority.

Field	Description
Bus Release	Determines how the EPC-1316 releases the VMEbus for other bus masters to use. You can select one of these: • **RONR (default)**: Release on No Request. Causes the EPC-1316 to release the VMEbus when its current bus access is complete. This has the effect of increasing the performance of other bus masters. • **RWD**: Release When Done. Causes the EPC-1316 to behave the same as RONR except it does not delay 50ns before trying to regain control of the bus. • **ROR**: Release on Request. Allows the EPC-1316 to perform better since it releases the VMEbus only if another bus master requests the bus.
VME ULA	Selects the unique logical address (ULA). Possible values range from 00 (default) through FF. This logical address is used to uniquely identify and access the EPC-1316 in a VXI system. To enter a value in this field, do one of these: • Enter a number from the keyboard • With NumLock enabled, enter a number from the keypad. • Press the space bar to increment the number. Note that there is no keystroke for decrementing a number.

Exit menu

Use the options in this menu to save and exit, or abandon your changes and exit to the system.

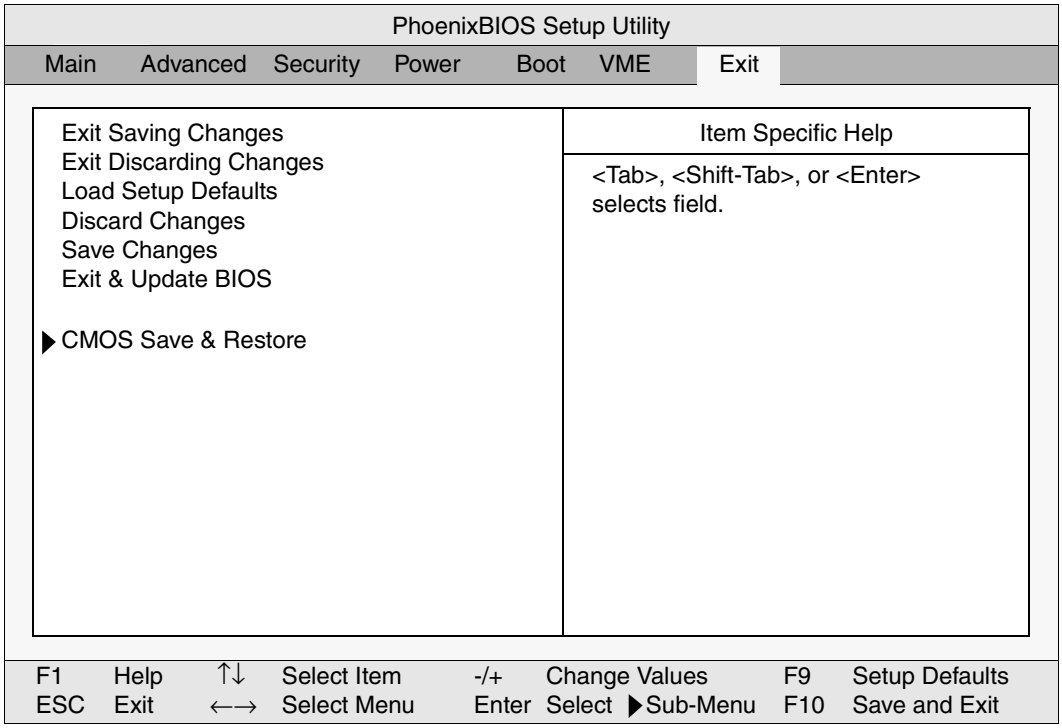


Figure 3-16. Exit menu

Field	Description
Exit Saving Changes	Saves the values you just entered and exits to load the operating system. The new values are loaded, and you exit and reboot.
Exit Discarding Changes	Discards the changes you just made and revert to the BIOS as it was before you entered the BIOS Setup program. The system boots with the old values.
Load Setup Values	Resets the BIOS values to the original, default values set at the factory, before any suppliers or other end users made changes.
Discard Changes	Loads the system with the previous values before this editing session started. You do not exit.
Save Changes	Saves the edits you made during this session but does not exit.

Field	Description
Exit & Update BIOS	Updates the BIOS from a floppy disk. **Note**: Select this exit option only if you obtained BIOS update replacement software from your supplier and reviewed the documentation and procedures provided with that distribution. This option changes the flash contents only if the vendor-supplied floppy is installed. If you select this option by mistake, changes made to the BIOS are lost unless already saved using the Save Current Values option. The system automatically seaches for the update program that should be on the floppy disk inserted in drive A. If no floppy exists, cycle power to reset the system to its previous state.
CMOS Save & Restore	Displays a menu that controls how the system handles CMOS values. For more information, see *CMOS Save and Restore sub-menu* on page 48.

CMOS Save and Restore sub-menu

Options in this menu specify how the system handles CMOS values.

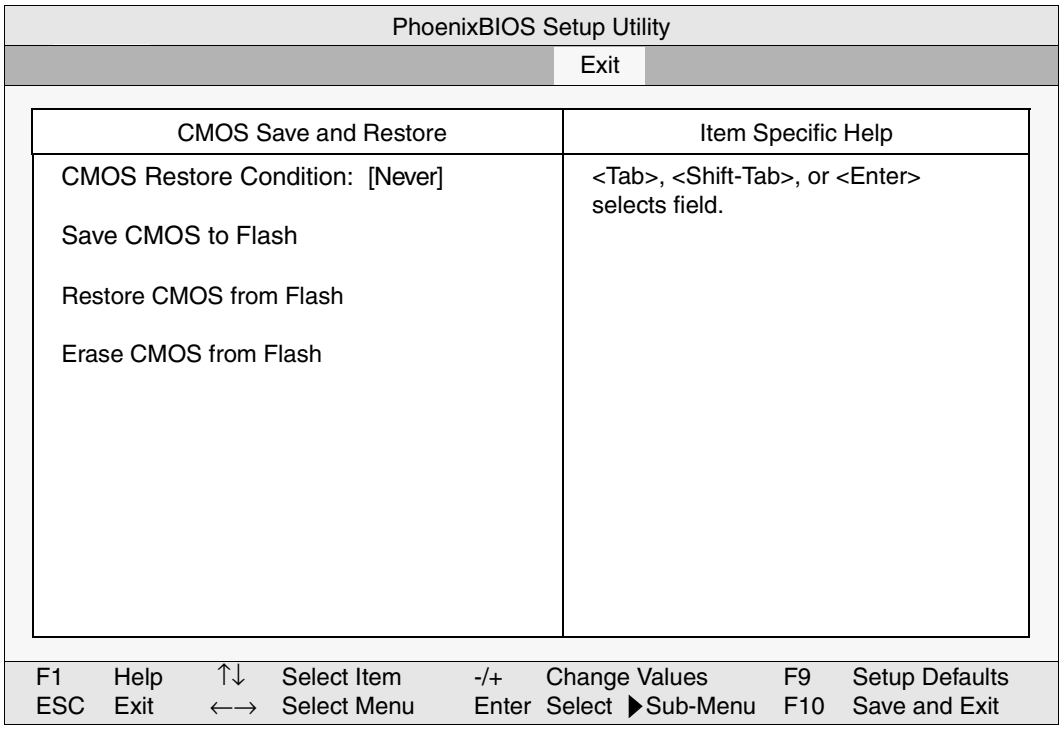

PhoenixBIOS Setup Utility
Exit
CMOS Save and Restore
Item Specific Help
CMOS Restore Condition: [Never]
Save CMOS to Flash
Restore CMOS from Flash
Erase CMOS from Flash
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

Figure 3-17. CMOS Save and Restore sub-menu

Field	Description
CMOS Restore Condition	Determines the conditions under which the BIOS restores CMOS RAM from FBD Parameter Block #1 when booting. You can select one of these: • Never (default) • CMOS Corruption • Always
Save CMOS to Flash	Immediately saves current settings in the Setup utility to CMOS RAM and into FBD Parameter Block #1. This process may take several seconds to complete. **Note**: Always select this option *before* restoring CMOS from Flash.
Restore CMOS from Flash	Immediately restores CMOS RAM and current settings in the Setup utility from FBD Parameter Block #1. **Note**: This option is available only if the CMOS was previously saved to Flash.
Erase CMOS from Flash	Immediately erases the CMOS image stored in the flash device.

4 Theory of operation

Overview

For information about RadiSys supplied EPC-1316 options, see the appropriate appendix:

- **MSIO Carrier Board**: *Appendix F, MSIO Carrier Board*
- **MSF option board**: *Appendix G, MSF option board*
- **Flash disk module**: *Appendix H, Flash disk module*.

For information about PMC modules, see the documentation that came with the module.

The EPC-1316 is a PCI/VME bus-compatible computer with standard PC peripherals, plus PCI and VME interfaces.

The EPC-1316's Main board is a 6U-sized board that contains a Mobile Pentium III processor including on board L1 and L2 cache, system memory, memory controller, a PCI/ISA/IDE bridge chip, a Flash Boot Device, a real-time clock, and a keyboard and mouse controller.

This board also contains these I/O functions: a Tundra Universe PCI/VME bridge, 10BASE-T or 100BASE-TX Ethernet, one RS-232 serial port, a Universal Serial Bus (USB) connector, and a connector for one PCI Mezzanine Card (PMC) that conforms to IEEE specification P1386.1 PMC, IDE/floppy/parallel interface via the P2 connector.

When reading this file online, you can immediately view information about any topic by placing the mouse cursor over a task and clicking.

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Figure 4-1 shows an overview of the system functional blocks. Most standard functions of the PC architecture are embodied in the Intel 82443BX PCI-based chipset. PC peripheral interfaces for monitor, keyboard, mouse, one serial ports, one Universal Serial Bus (USB) port, a PMC module, and an RJ-45 Ethernet connector are provided at the front panel. An external floppy drive can be attached via the P2 connector for installing software and loading and updating flash ROM BIOS and BIOS extensions. If the MSI/O card is fitted, then the EXP-FDM interface can be alternatively used for BIOS updates. A Phoenix NuBIOS with flash update capability allows updating the System BIOS and addition of BIOS extensions. A watchdog timer is also provided.

The VMEbus interface uses the Tundra Universe PCI/VME bridge and includes special PAL-based VME byte-order swapping hardware to deal with the difference between Intel and Motorola data representations. Byte-swapping of D16 and D32 accesses only occurs when desired, and is configureable via the Universe register.

EPC-1316 organization

Block diagram

The block diagram in the next figure shows the division and interconnection of EPC-1316 functions. These are described in the following sections.

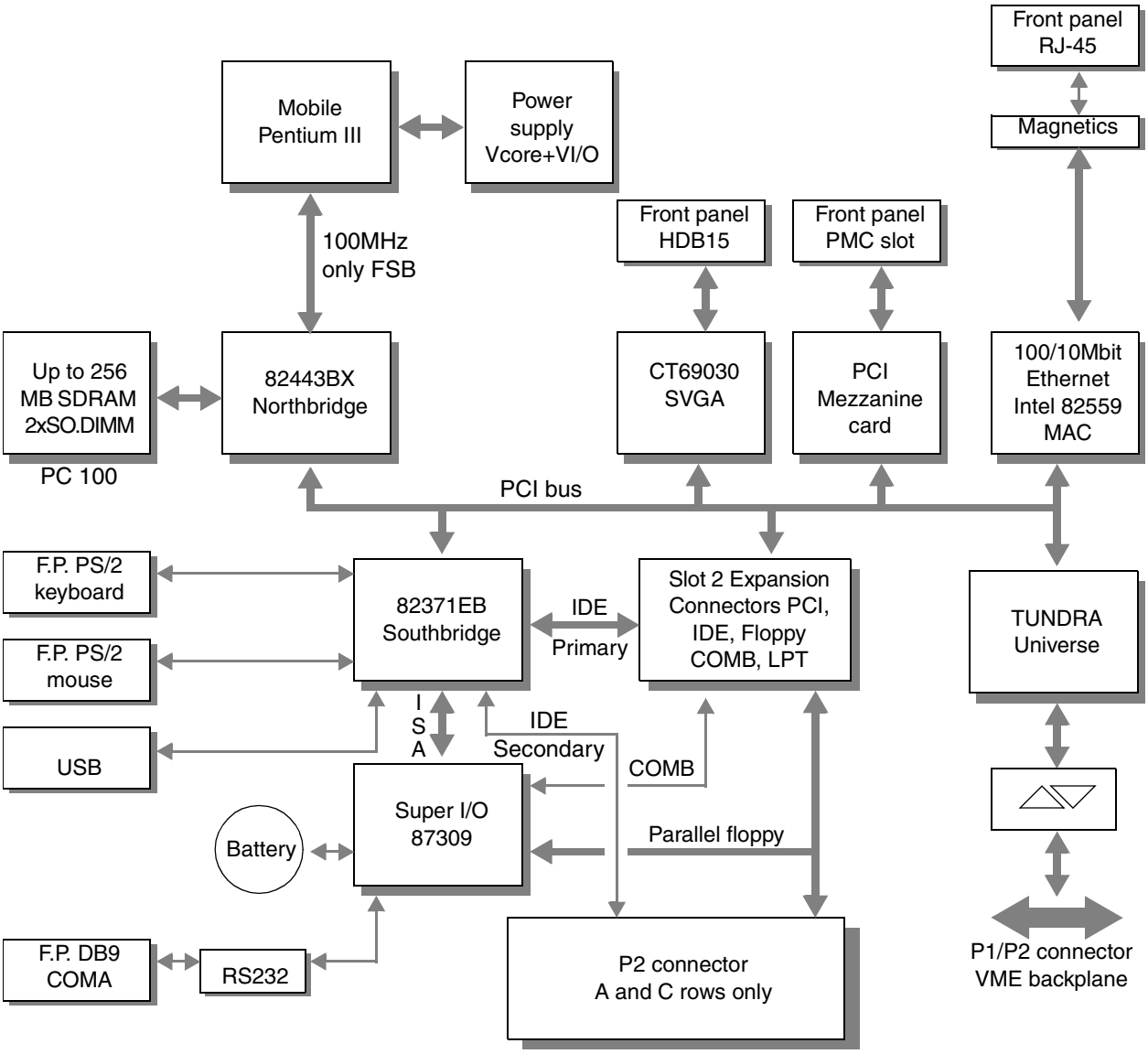


Figure 4-1. Block diagram: EPC-1316

Features

Processor

An Intel Mobile Pentium III processor (with integral FPU) runs at 400 MHz. The processor, the system controller, and SDRAM all operate on a 100MHz local bus. The PCIbus runs at (33MHz) and the ISA bus runs at one quarter the PCI bus speed (8.33 MHz).

Cache memory

A second-level (L2) write-back 256KByte main-memory cache is included internally to the Pentium III processor. It runs at the full local bus frequency.

Main system memory

Main memory is implemented as SODIMM 144-pin socketed 3.3 volt unbuffered SDRAM. The EPC-1316 supports up to 256MB of PC100 SDRAM in two 144-pin SODIMM sockets. The 443BX controller generates all of the required control signals, such as ~RAS, ~CAS, and ~WE, as well as the multiplexed addresses for the SDRAM array.

Memory map

The 2^{32} byte physical address space seen by the Intel Pentium occupies three areas:

1. The area between 0 and 1 MB is largely defined by the IBM PC/AT architecture.
2. The area between 1 MB and 256 MB depends on how much DRAM is installed in the EPC-1316.
3. The area above 256 MB, provides direct mapping to the VMEbus with a variety of address modifiers and byte orderings.

Memory at addresses between 0 and 1 MB (000FFFFFh) is mapped as follows:

Range	Content
00000000h–0009FFFFh	DRAM
000A0000h–000BFFFFh	VGA framebuffer
000C0000h–000CAFFFh	Shadowed VGA BIOS
000CB000h–000CFFFFh	Reserved
000D0000h–000D3FFFh	Universe registers
000E4000h–000EFFFFh	Shadowed system BIOS
00100000h–07FFFFFFh	DRAM. If no DRAM exists, ISA memory
10000000h–1XXXFFFFh	Reserved
80000000h–BFFFFFFFh	VME A32
CXXX0000h–DXXXFFFFh	VME A16
EX000000h–EXFFFFFFh	VME A24
F0000000h–FFF7FFFFh	Reserved
FFF00000h–FFFFFFFFh	System BIOS

PCI resources

Table 4-1. EPC-1316 device ~IDSEL assignments

Number	Device	IDSEL	INT	REQ/GNT
0	443BX	AD11	N/A	N/A
1	AGP bridge	AD12	N/A	N/A
2	Ethernet	AD13	C	0
3	PMC	AD14	B	1
4	Universe II	AD15	D	2
5	SCSI	AD16	A	3
6	PCI/PCI bridge	AD17	N/A	N/A
7	PIIX4	AD18	N/A	N/A
8	C&T 69030	AD19	A	N/A

Ethernet controller

The EPC-1316 implements 10/100BASE-T Ethernet communications by using the Intel 82559 10BASE-T and 100BASE-TX Ethernet Controller. The 82559 chip interfaces to the 32-bit PCIEPC-1316 device ~IDSEL assignments bus and receiver for a 10BASE-T and 100BASE-TX Fast Ethernet connection to Category 5 unshielded twisted-pair cable via an RJ45 connector.

The Ethernet controller uses INTC and Bus Arbitration channel 0, which is configured through the PCI configuration space. It is implemented as device 2 for host PCI bus configuration space accesses (IDSEL = AD13).

Video controller

The EPC-1316 hardware includes a VGA graphics controller implemented using the Chips and Technologies CT69030 GUI-Accelerated VGA/XGA. This is connected to the local PCI bus to give the best possible graphics performance and controls an SVGA/XGA monitor connected to the VGA front panel connector. The CT69030 is located as device 8 (IDSEL = AD19) for host PCI bus configuration space accesses. The CT69030 has on-chip frame buffer memory, providing 4MBytes of video memory which results in these resolutions:

Table 4-1. Windows 95 video driver capability

Resolution	Colors	Refresh rates (Hz)
640 x 480	256, 64K, or 16M colors	Refresh set to *Optimal and Default*
800 x 600	256, 64K, or 16M colors	Refresh set to *Optimal and Default*
1024 x 768	256 or 64K colors	Refresh set to *Optimal and Default*
1280 x 1024	256 colors	Refresh set to *Optimal and Default*
1600 x 1200	256 colors	Not available

Table 4-2. Windows 98 video driver capability

Resolution	Colors	Refresh rates (Hz)
640 x 480	256, 64K, or 16M colors	Not available
800 x 600	256, 64K, or 16M colors	Not available

Table 4-2. Windows 98 video driver capability

Resolution	Colors	Refresh rates (Hz)
1024 x 768	256 or 64K colors	Not available
1280 x 1024	256 colors	Not available
1600 x 1200	256 colors	Not available

Table 4-3. Windows NT video driver capability

Resolution	Colors	Refresh rates (Hz)
640 x 480	256, 64K, or 16M colors	60, 75, 85, 100
800 x 600	256, 64K, or 16M colors	60, 75, 85, 100
1024 x 768	256 or 64K colors	60, 75, 85
1280 x 1024	256 colors	60, 75
1600 x 1200	256 colors	60

Flash boot device

The Intel E28F800B5-T is used as a Flash Boot Device (FBD). This is flash-updatable BIOS containing the boot, main, and parameter blocks shown in Figure 4-2 and shadowed at the top of 32-bit address space. The use of the FBD allows reprogramming of the main and parameter blocks of the BIOS.

The Plug-and-Play ESCD is also stored in the Boot-Block FLASH device in the block addressed from FFFFA000h–FFFFBFFFh. This block is always accessible for re-programming.

Use extreme caution when re-programming the flash chip. The Boot Block rarely changes and should not require re-programming, even when the main and parameter blocks are reprogrammed. The capability to program the boot block is provided only to facilitate changes by RadiSys during manufacturing.

A force recovery jumper is provided and is connected to a G-PI pin on the PIIX4E. This jumper is readable by the boot block and can force the boot block to initiate a recovery sequence at power-up should other methods of initiating the sequence, such as crisis recovery, become inaccessible.

The Flash BIOS device is memory addressed and resides in the last 1MB of system memory at address FFF00000h–FFFFFFFFh.

BIOS ROM and ROM shadowing

The EPC-1316 utilizes a Flash Boot Device (FBD) as its BIOS ROM. The BIOS ROM is mapped into the top of the processor's 32-bit address space. The BIOS consists of a 16 KByte boot block and the System BIOS in the 96KB main block and both 8KB parameter blocks. The layout is described in the next figure.

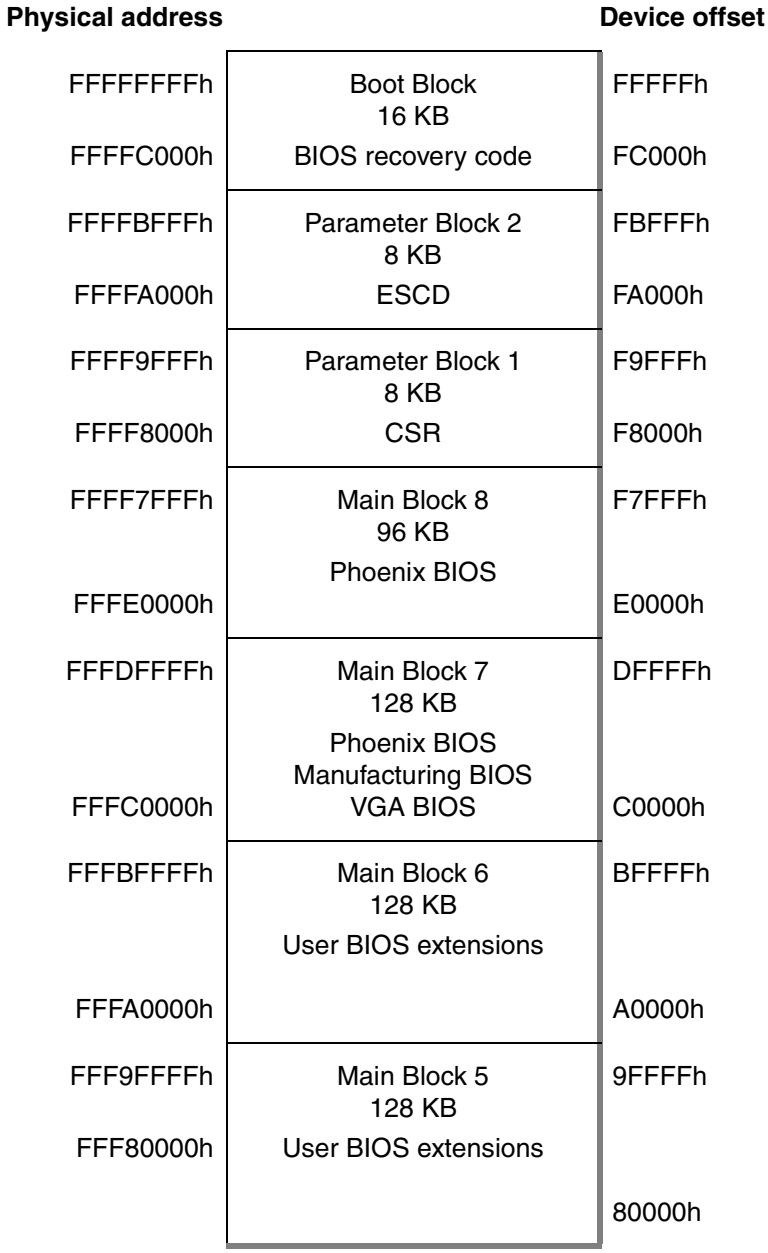


Figure 4-2. Flash boot device memory: upper 512 KB

The BIOS initialization software copies the ROM contents into DRAM (a process called *shadowing*) at addresses 0E0000h–0FFFFFh. The VGA BIOS is copied into 0C0000h–0C7FFFh of DRAM. After copying into these areas, the BIOS write-protects them. Subsequent writes to these areas complete successfully but do not alter the data in DRAM.

There are two parameter blocks, each 8 KB in size, used for BIOS code.

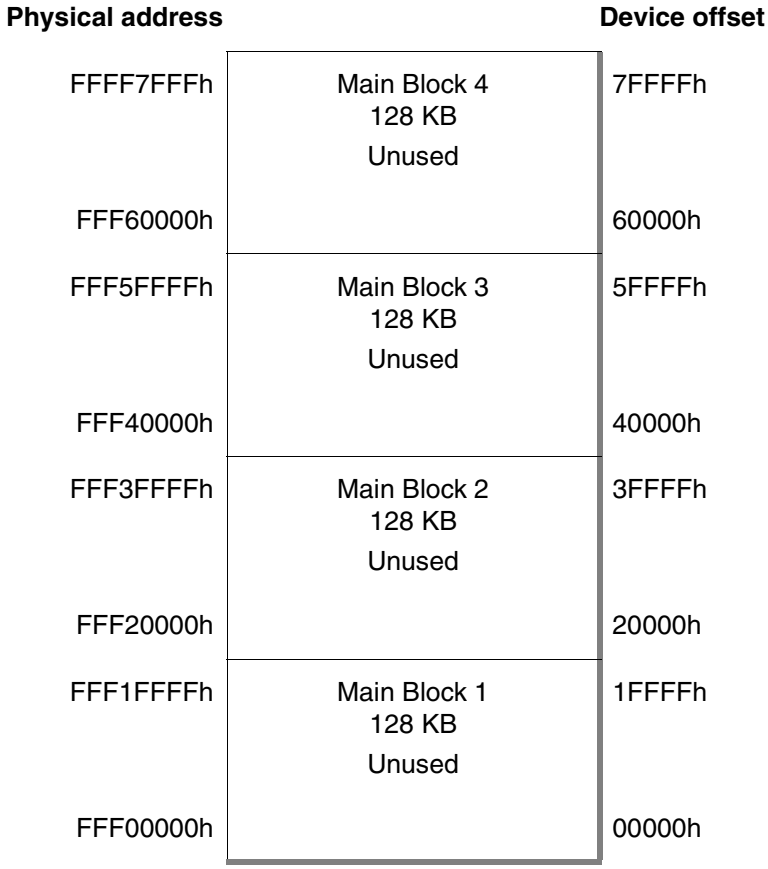


Figure 4-3. Flash boot device memory: lower 512 KB

Keyboard/mouse controller

The mouse/keyboard controller is integrated into the National Semiconductor 87309 Super I/O chipset. This controller can interface to most standard PC mice and keyboards with PS/2-style connectors. The keyboard controller uses interrupt IRQ1 and the mouse uses IRQ12.

CMOS backup and restore

CMOS memory is backed up to and restored from Parameter Block 1 of the FBD, as determined by the settings in the BIOS Setup Exit Menu. This allows you to save settings to nonvolatile flash memory and to specify the conditions under which to restore CMOS from the FBD. For more information, see the Exit menu in *Chapter 3, BIOS configuration*.

Battery

The battery powers the CMOS RAM and TOD clock when system power is not present. At 60°C, the battery should have a life of over four years. In a system that is powered on much of the time and where the ambient power-off temperature is less than 60°C, the battery is estimated to have a life of 10 years.

If system power is present, the +5V voltage also powers the CMOS RAM and TOD clock. This is done with the RTC chip's internal isolation diodes, so that either the onboard battery or the +5V power supply voltage can supply power, and neither power source affects the other.

The 3.0V 200mA Hr lithium battery supplied with the EPC-1316 is a 28mm CR2032 "coin cell" or equivalent. It is mounted at the rear of the Main I/O Board. Should the battery fail, you can obtain and install a replacement.

For information about replacing the battery, see *Replacing the battery* on page 14 .

Watchdog timer

The watchdog timer is a binary counter which, upon overflow, signals a watchdog timer event. The counter causes a watchdog event after approximately 125 ms, 1 second, or 8 seconds (depending on the value of WDTV, bits 2 and 1 in register 8150h) if the application software does not reset the timer.

An I/O read to address 8150h resets the counter. If WDTR (bit 3 of register 8150h) is set, the following occurs in response to a timeout event:

A watchdog hardware reset results in a "warm" hardware reset, which clears WDTR (bit 0 of the Module Status) to allow the hardware to be released from the warm reset state. SYSFAIL continues to be driven until the WDTIE bit is cleared by either reading the Module Status/Control Register or by a power-on reset.

The "warm" hardware reset does not clear the following:

- **The upper four bits of the Configuration register**: control Slot-1 arbitration functions.
- **Bit 4 of the Module Status/Control register**: enables the VME bus time-out function and
- **Bit 6 of the Module Status/Control register**: enables asserting ~VME SYSRESET, if set.

- If WDTR is clear, WDTIE mask (bit 0 of register 8153h) enables an interrupt if a time-out event occurs (SYSFAIL is not driven).
- The clock input to the counter is disabled if the interrupt is pending and not serviced.
- Service of the interrupt is signaled to the counter by reading register 8150h. This resets the counter value and resumes counting.
- The interrupt is signaled on IRQ10.
- The timer event also clears WDTIE bit in the VME event register (bit 0 of register 8153h).

Application software that uses this timer should take care to reset the counter just prior to enabling the interrupt bit in register 8155h. This inhibits a spurious timer event from occurring just after enabling the timer.

Peripheral ports

The I/O address and IRQ of peripheral ports are determined by the CMOS parameters established by default. This includes one serial port (RS-232 (COM A)), a bi-directional

parallel port. The COM A or COM B ports and the parallel port, along with the floppy disk controller, are implemented by the National 87309 Super I/O Chip.

RS-232 ports

The RS-232 ports are standard PC COM serial ports based on the 16550 architecture. COM A is normally mapped to I/O address 3F8h–3FFh and uses interrupt IRQ4.

If not needed, COM A can be disabled in the BIOS Setup Integrated Peripherals Sub-Menu to free up the I/O address and interrupt for usage by other expansion products.

USB port

The Universal Serial Bus (USB) controller is a host controller that moves data between the main system memory and devices on the serial bus. If more than one device is required, an external hub can be connected to the USB port.

USB architecture has the concept of all devices connected to it being serviced through two software layers known as SBS (serial bus services) and UHCS (universal host controller services). SBS allocates the necessary bandwidth for every device connected on the bus and builds a scheduler to service these devices at the required intervals. SBS passes the schedule information to the UHCS layer. The UHCS uses this information to build a schedule table and command blocks that hardware understands. The schedule table and command blocks are located in the system memory and contain information including the addresses for data movements to/from system memory. The current implementation of the USB support software may not support these features at initial product availability.

A host-side USB port is provided on the front panel. The USB's PCI configuration registers are located as function 2 of the PIIX4 configuration space. The PIIX4E supports first level hub functions but the EPC-1316 cannot utilize this as only one port is available.

IDE ports

Two IDE interfaces are available from the PIIX4E device, the primary IDE is used by the MSI/O card and the secondary IDE port can be utilized via the P2 backplane connector.

PCI/VME bridge

The VMEbus interface on the EPC-1316 is controlled by a single chip: the Tundra Semiconductor, Universe PCI/VME bridge. The Universe chip controls a layer of buffers between it and the VMEbus, and has a glueless interface to the PCIbus.

The VMEbus interface uses both the P1 and P2 connectors to allow an addressing space of A16/A24/A32 with D08/D16, D32, and D64 data accesses. It uses PCI INTD and bus mastering lines. The VME bus interface includes the following features:

- RE/GNT2, located as device #4 (IDSEL=AD15).
- Full VMEbus System Controller (Slot 1) features including bus arbiter, bus timeout, IACK daisy chain driver, SYSCLK driver.
- Master control in A16/A24/A32 address spaces for D08/D16 and D32 data widths.
- Responds as D08/D16 and D32 slave in A16/A24/A32 address spaces.
- Generates and responds to all seven VMEbus interrupts.

- Can access VME registers from either the Pentium or VMEbus.

The EPC-1316 presents a single load on all VMEbus signals.

For more information about programming the VMEbus interface, see *Chapter 5, Programming the VMEbus interface*.

Resetting the EPC-1316

This section describes various methods to reset (reboot) the EPC-1316.

Power-off, power-on

"Cold" hardware reset. This causes all boards in the VMEbus to reset. The system runs the power-on self-test and reboots the OS.

Power low

"Warm" hardware reset. When power is detected below ~4.5V, the system performs a cold hardware reset.

Front panel Reset button

"Cold" hardware reset. The Reset button causes the EPC-1316 to perform a hardware reset The system runs the power-on self-tests and reboots the operating system.

Ctrl+Alt+Del

"Warm" software reset. This keyboard sequence is also called a "warm boot". The EPC-1316 does not reinitialize all of the processor's hardware. However, the operating system reloads.

VMEbus SYSRESET

"Warm" hardware reset. The EPC-1316 can be software-configured to respond or not respond to the VMEbus ~SYSRESET line. Asserting bit 7(SRIE) of register 8144h allows the ~VME SYSRESET signal to reset the EPC-1316. The reset semantics are the same as the front panel reset.

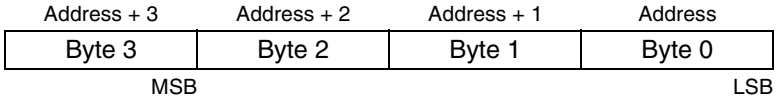
Watchdog timer

"Warm" hardware reset. Same as a front panel reset button except that SYSFAIL is asserted until the watchdog timer is cleared.

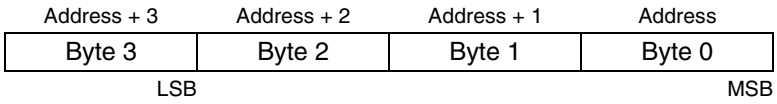
Notes on byte ordering

There are two fundamentally different ways of storing numerical values in byte locations in memory:

- Little endian, characteristic of Intel microprocessors, where the *least*-significant data byte (LSB) is stored in the lowest byte address.



- Big endian, characteristic of Motorola microprocessors and the VMEbus environment in general, where the *most*-significant data byte (MSB) is stored in the lowest byte address.



The EPC-1316 contains programmable byte-swapping hardware to allow programs to read or write VMEbus memory in either byte order. The EPC-1316 uses the Tundra Universe supervisor address modifier bit, AM bit 2, to control byte-swapping. This bit is emitted by the Universe chip and intercepted by the EPC-1316 byte-swap control hardware which uses it to control whether or not byte-swapping occurs. The EPC-1316 always asserts AM bit 2 to the VMEbus, so only supervisor accesses are possible.

The four slave images written to VMEbus memory are controlled by setting the Universe chip's SUPER bitfield (bit 12) of the four Target Image Control Registers (LSI0_CTL through LSI3_CTL). You can set SUPER to the following values:

zero — Non-privileged mode. Enables swapping, producing a Motorola (big-endian) image.

one — Super mode. Disables swapping, producing an Intel (little-endian) image.

You use little-endian images to map VMEbus memory to another Intel processor and big-endian images to map VMEbus memory to a Motorola processor.

For details about the Slave Image Control Registers, access the *Universe User Manual* as described in *For more programming information* on page 66.

The particular control registers for each image are described in *Appendix A, Chipset and I/O map*.

Slave image control register	Offset
LSI0_CTL	100h
LSI1_CTL	114h
LSI2_CTL	128h
LSI3_CTL	13Ch

When you perform a single byte (D08) access, the byte order makes no difference. However, word (D16) or double-word (D32) accesses may require byte-swapping.

When you select little-endian, bytes pass straight through unchanged. You should only use little endian when you read or write data between two Intel processor systems. The result of using little-endian byte ordering to transfer a double-word integer between an Intel processor and a Motorola processor are shown below.

Since the Pentium processor uses Addr as the least-significant byte and the Motorola processor uses Addr as the most-significant byte, the processor receiving the data gets a "scrambled" value.

When big-endian is selected, the bytes are swapped between the Pentium and VME:

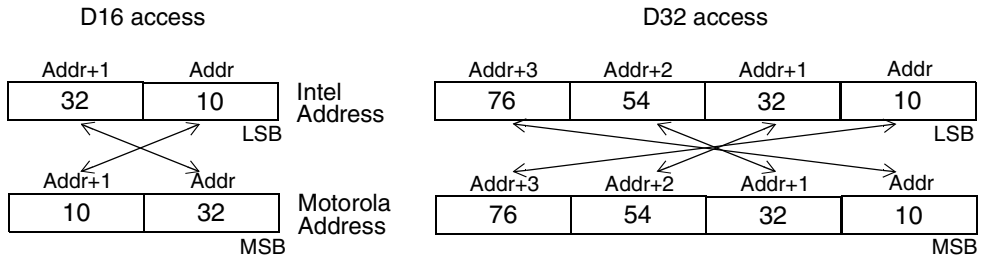


Figure 4-4. Using big-endian byte ordering

When using big-endian byte ordering, take care to ensure that the VME address is aligned on a boundary. For D16 accesses, the VME address must be on a word boundary (address evenly divisible by 2). For D32 accesses, the VME address must be on a double-word boundary (evenly divisible by 4). Failure to properly align addresses results in "scrambled" data. Although the VMEbus address must be boundary-aligned to match the data width (word or double-word), the Pentium address does not need to be boundary-aligned.

You must also consider the compiler you are using, because some compilers produce two 16-bit accesses when a 32-bit access is desired, resulting in scrambled data.

When transferring a 32-bit floating-point number, take care to assure that both processors use the same floating-point format and that both systems expect the mantissa and exponent in the same byte locations. As long as these match, floating-point number transfers work correctly. Since 64-bit floating-point number transfers are not supported in hardware, use two 32-bit transfers with little-endian byte order and then accomplish the byte-swap in software.

The EPConnect Bus Manager software provides a means of selecting the byte ordering during memory-copy operations.

When using D64 data widths on the VMEbus:

- Use only Supervisor (non-swapped) mode. Byte-swapping using the non-priviledged mode does not work correctly
- Use only little-endian byte ordering. In 64-bit data bus mode, only little-endian byte ordering is allowed.

5 Programming the VMEbus interface

The VMEbus is controlled by the Tundra Universe PCI-VME bridge chip. Active access to the VMEbus is achieved by reading and writing to registers in the Universe memory space. Because of dependencies between the PCI and VME sides of those registers which are ported to both buses, considerable care must be exercised in both reading and writing to these registers.

For all but the most basic programming, try using the programming interface provided by EPConnect software instead of working directly with the VMEbus registers. For more information about EPConnect, a C/C++ programming interface to the Microsoft Windows NT API, see the *EPConnect for Windows NT/4.0 Programmer's Reference Guide*, available from Radisys.

Register initialization

At power-on-self-test (POST) time, a subset of the VME registers is initialized by the BIOS. The Universe chip then initializes the remainder of the VME registers. This is controlled by how the Universe chip is programmed.

Programming the Universe chip

The Universe chip can become system controller if the EPC-1316 is in Slot 1. It does this by sampling the VME signal ~BG3IN. If BG[3:0] is low after reset, which it is due to the Universe chip's internal pull-down, then the EPC-1316 is in Slot 1 and the Universe chip becomes system controller. When the Universe is the System Controller, its IACK daisy chain driver and SYSCLK driver are also activated.

VMEbus arbiter

The bus arbiter supports the following arbitration modes:

- Fixed Priority Arbitration (PRI).
- Single Level arbitration (SGL), a subset of PRI.
- Round Robin arbitration (RRS), the default setting.

The arbitration mode is selected in the Universe MISC_CTL register. The arbiter can be programmed to time out if the requester does not assert ~BBSY within a specified period. The timeout can be set to 16 µs (default), 256 µs, or disabled via the MISC_CTL register.

VMEbus timer

A programmable bus timer allows the VMEbus timeout period to be selected via the MISC_CTL register. It can be programmed to 16 µs, 32 µs, 64 µs (default), 128 µs, 256 µs, 512 µs, 1024 µs, or Disabled. If a bus transaction times out, the timer asserts the VMEbus ~BERR signal.

VMEbus requester

The Universe chip is software-configurable to request bus ownership on all VMEbus request levels: ~BR3 (default request level), ~BR2, ~BR1, and ~BR0. Demand Mode is the default request mode.

The VMEbus requester can be configured in either Release-When-Done (RWD; default) or Release-On-Request (ROR) mode.

VMEbus master accesses

The EPC-1316 becomes VMEbus Master in the following situations:

- The Pentium accesses resources on the VMEbus.
- The Universe DMA controller performs block-transfer operations.
- The Universe generates interrupt-acknowledge cycles as the VMEbus interrupt handler.
- The Universe VMEbus ownership bit (VOWN in the MSTR_CTL register) is set.

The board can perform master accesses in A16, A24 and A32 address spaces using D08/D16/D32, and D64 data widths. Read accesses to the VMEbus are always coupled, while write accesses may either be posted or coupled. Write accesses default to coupled.

The Universe provides four programmable windows into VMEbus memory (PCI Slave images). The characteristics of the these windows are programmed in the LSIn_CTL, LSIn_BS, LSIn_BD, and LSIn_TO registers of the Universe chip. For programming details, access the *Universe User Manual* as described in For more programming information on page 66.

VMEbus block transfers are supported by the Universe using its on-chip DMA controller.

The EPC-1316 can respond as a VMEbus Slave in either A24 or A32 address spaces. It responds to either D08, D16, D32, or D64 accesses. Read accesses from the VMEbus to onboard memory may be either coupled or prefetched (for block transfers), while write accesses may either be posted or coupled. Both reads and writes default to coupled.

The Universe provides four programmable windows into PCI memory (VME Slave images). The characteristics of the these windows are programmed in the VSIn_CTL, VSIn_BS, VSIn_BD, and VSIn_TO registers of the Universe chip. For programming details, access the *Universe User Manual* as described in For more programming information on page 66.

By default, none of the Universe slave images are used or programmed in the EPC-1316.

VMEbus locked accesses (RMW)

Each of the four PCI Slave images support VMEbus Read-Modify-Write (RMW) cycles, if so programmed. This causes a non-block VMEbus RMW read cycle to generate a coupled PCI locked read cycle. PCI ~LOCK is then asserted on the PCI bus until ~AS is negated on the VMEbus.

VMEbus interrupter

The Universe VME controller provides a flexible scheme to map interrupts to either the PCI bus or the VMEbus. This mapping is controlled in the LINT_EN, LINT_MAP0, LINT_MAP1, VINT_EN, VINT_MAP0, and VINT_MAP1 registers.

The following interrupts can be mapped to any VMEbus ~IRQ pins.

- PCI bus errors
- VMEbus errors
- DMA interrupts
- Software interrupts

If a software and a hardware source are both mapped to the same ~IRQ, the software source has higher priority.

When an IACK cycle on the VMEbus is detected that matches an interrupt level that the EPC-1316 is asserting (and the IACKIN daisy chain is asserted into the EPC-1316), the Universe responds by supplying an 8-bit STATUS/ID vector. This vector is programmable through the STATID register. When the IACK cycle is complete, the Universe releases the VMEbus and the interrupt vector is passed to the PCI master (Pentium). Software interrupts are Release-On-Acknowledge (ROAK), while hardware and internal interrupts are Release-On-Register-Access (RORA).

VMEbus access to Universe registers

As mentioned earlier, the Universe chip can be programmed to make its registers accessible from the VMEbus. The Universe powers up with VMEbus access to its registers disabled, and it can be later programmed by application software to enable them for VMEbus access. This functionality is controlled by programming the VRAI_CTL and VRAI_BS registers.

PCIbus access to Universe registers

The Universe chip is defined as a PCI device, therefore it must provide a standard set of 64 DWORD-wide registers within the PCI Configuration Space. They are selected by asserting the Universe IDSEL DB signal on a Configuration Space access. Since the Universe registers consume a 4K block of memory, only the first 256 registers can be accessed through Configuration Space. The remaining registers must be accessed through memory or I/O space.

This 4KB block is also larger than the available area left in the I/O space. Therefore, the registers are memory mapped. The base address of the registers must reside on a 64KB

boundary, so they are placed at D0000h. The entire register set is accessible in the D0000h–D3FFFh range.

For more programming information

For complete programming information about the Tundra Universe chip, see the most current version of the *Universe User Manual*, available online at this URL:

`http://www.tundra.com/unidex.html`

A Chipset and I/O map

The following defines the I/O addresses decoded by the EPC-1316. Only the A9–A0 bits are decoded for the registers between 200h and 3FFh. For the I/O addresses above 8000h, A15 and A9–A0 are decoded.

First (8-bit) DMA controller

I/O Addr	Usage
000	Channel 0 address
001	Channel 0 count
002	Channel 1 address
003	Channel 1 count
004	Channel 2 address
005	Channel 2 count
006	Channel 3 address
007	Channel 3 count
008	Command/status
009	DMA request
00A	Command register (R) Single-bit DMA request mask (W)
00B	Mode
00C	Set byte pointer (R) Clear byte pointer (W)
00D	Temporary register (R) Master clear (W)
00E	Clear mode register counter (R) Clear all DMA request mask(W)
00F	All DMA request mask

First interrupt controller

I/O Addr	Usage
020	Port 0
021	Port 1

Counter-timer functions

I/O Addr	Usage
040	Counter 0
041	Counter 1

I/O Addr	Usage
042	Counter 2
043	Control (W)

Keyboard controller and port

I/O Addr	Usage
060	Data I/O register
061	Chipset port B register
064	Command/status register

Time-of-day clock

I/O Addr	Usage	
070	RTC index register	
071	RTC data register	
	0	seconds
	1	seconds alarm
	2	minutes
	3	minutes alarm
	4	hours
	5	hours alarm
	6	day of week
	7	date of month
	8	month
	9	year
	A	status A
	B	status B
	C	status C
	D	status D
	E...3F	RAM

Phoenix NuBIOS

I/O Addr	Usage
080	Phoenix BIOS status information

DMA page registers: Intel EX 82371EB of PC/AT

I/O Addr	Usage
081	Channel 2 page register
082	Channel 3 page register
083	Channel 1 page register
087	Channel 0 page register
089	Channel 6 page register
08A	Channel 7 page register

I/O Addr	Usage
08B	Channel 5 page register
08F	Refresh page register

Port A

I/O Addr	Usage
092	Fast A20 and reset control

Second interrupt controller

I/O Addr	Usage
0A0	Port 0
0A1	Port 1

Power management controller

I/O Addr	Usage
0B2	Control
0B3	Status

Second (16-bit) DMA controller

I/O Addr	Usage
0C0	Channel 4 address
0C2	Channel 4 count
0C4	Channel 5 address
0C6	Channel 5 count
0C8	Channel 6 address
0CA	Channel 6 count
0CC	Channel 7 address
0CE	Channel 7 count
0D0	Command/status
0D2	DMA request
0D4	Command register (R) Single-bit DMA request mask (W)
0D6	Mode
0D8	Set byte pointer (R) Clear byte pointer (W)
0DA	Temporary register (R) Master clear (W)
0DC	Clear mode register counter (R) Clear all DMA request mask (W)
0DE	All DMA request mask
0E0	Phoenix BIOS status information

Coprocessor interface

I/O Addr	Usage
0F0	Clear coprocessor busy
0F1	Reset coprocessor
15C	Super I/O 87309 interface index register
15D	Super I/O 87309 interface data register

IDE control

I/O Addr	Usage
1F0	Data
1F1	Error/features
1F2	Sector count
1F3	Sector number
1F4	Cylinder low
1F5	Cylinder high
1F6	Drive/head
1F7	Status/command

ISA Plug and Play control

I/O Addr	Usage
279	
A79	Data register
CF8	Configuration address register
CF9	Turbo reset control register
CFC	Configuration data register

Serial I/O (COM B) port

I/O Addr	Usage
2F8	Receiver/transmitter buffer (only if EPC-1316 includes the MSIO option) Baud rate divisor latch (LSB)
2F9	Interrupt enable register Baud rate divisor latch (MSB)
2FA	Interrupt ID register
2FB	Line control register
2FC	Modem control register
2FD	Line status register
2FE	Modem status register

Parallel I/O (LPT1) port

I/O Addr	Usage
378	Printer data register
379	Printer status register
37A	Printer control register

EPP registers

I/O Addr	Usage
37B	EPP address port
37C	EPP data port 0
37D	EPP data port 1
37E	EPP data port 2
37F	EPP data port 3

VGA

I/O Addr	Usage
3B4	CRT controller index
3B5	CRT controller data
3BA	Feature control output, input status
3C0	Attribute controller index/data
3C1	Attribute controller index/data
3C2	Miscellaneous output, input status
3C4	Sequencer index
3C5	Sequencer data
3C6	Video DAC pixel mask, hidden DAC register
3C7	Pixel address read mode, DAC state
3C8	Pixel mask write mode
3C9	Pixel data
3CA	Feature control readback
3CC	Miscellaneous output readback
3CE	Graphics controller index
3CF	Graphics controller data
3D0–D3	Reserved for VBA controller
3D4	CRT controller index (CGA emulation)
3D5	CRT controller data (CGA emulation)
3D6	Configuration extensions index
3D7	Configuration extensions data
3DA	Feature control, input status

Serial I/O (COM A) port

I/O Addr	Usage
3F8	Receiver/transmitter buffer Baud rate divisor latch (LSB)
3F9	Interrupt enable register Baud rate divisor latch (MSB)
3FA	Interrupt ID register
3FB	Line control register
3FC	Modem control register
3FD	Line status register
3FE	Modem status register

First interrupt controller: Intel EX 82371EB of PC/AT

I/O Addr	Usage
4D0	Edge/level control—INT1
4D1	Edge/level control—INT2

ISA Plug and Play

I/O Addr	Usage
778	FIFO
779	Configuration Register B
77A	Extended Control Register

ISA Plug and Play

I/O Addr	Usage
A79	Data register
CF8	Configuration address register
CF9	Turbo reset control register
CFC	Configuration data register

VME and miscellaneous registers

I/O Addr	Usage
814C–814D	Message high register
814E–814F	Message low register
8150	Control
8151	ULA register
8152	VME event state register
8153	VME event enable register
8154–8155	Status/control register
8156	Model register
8158–8159	Signal FIFO register
8162–8163	IACK latch 1 register

I/O Addr	Usage
8164–8165	IACK latch 2 register
8166–8167	IACK latch 3 register
8168–8169	IACK latch 4 register
816A–816B	IACK latch 5 register
816C–816D	IACK latch 6 register
816E–816F	IACK latch 7 register

ULA relative VXI registers within VME address space

I/O Addr	Usage
0–1	ID/ULA register
2–3	Device type register
4–5	Status/control register
6–7	Reserved
8–9	Protocol register
A–B	Response register
C–D	Reserved
E–F	Message register

B Interrupts

Interrupts

The following table shows interrupt assignments for the EPC-1316.

Table B-1. Interrupts

Interrupt	Description
IRQ0	Timer
IRQ1	Keyboard controller
IRQ2	Cascade interrupt input
IRQ3	COM B serial port, if enabled
IRQ4	COM A serial port, if enabled
IRQ5	Unassigned
IRQ6	Floppy disk controller, if enabled
IRQ7	LPT1 parallel port, if enabled
IRQ8	Real-time clock
IRQ9	Unassigned
IRQ10	VXI interrupts
IRQ11	Unassigned
IRQ12	Mouse, if enabled
IRQ13	Numeric coprocessor
IRQ14	Primary IDE, if enabled
IRQ15	Secondary IDE, if enabled
NMI	PIIX4E NMI
SMI	Power management
PIRQA	Graphics, optional SCSI
PIRQB	Ethernet
PIRQC	PMC site
PIRQD	PIIX4E, Universe Bridge (one of 11 VME events): 7 VME interrupts, VME ACFAIL, VME SYSFAIL, VME BERR, Watchdog timer event. (mapped to IRQ10)

DMA Channels

The following table shows DMA channel assignment for the EPC-1316.

Table B-2. DMA channels

Channel	Assignment
0	Unassigned (8-bit)
1	Unassigned (8-bit)
2	Usually needed for floppy disk (8-bit)
3	Unassigned (8-bit)
4	(Channel 0–Channel 3 cascade through Channel 4)
5	Unassigned (16-bit)
6	Unassigned (16-bit)
7	Unassigned (16-bit)

C Connectors

This appendix specifies the details of the connectors and jumpers used on the EPC-1316.

For information about connectors on optional boards and modules, see the appropriate appendix:

- *Appendix F, MSIO Carrier Board*
- *Appendix G, MSF option board*
- *Appendix H, Flash disk module*
- *Appendix I, PMC modules*

This product includes the connectors and jumpers listed in the table below. When reading this file online, you can immediately view information about any connector by placing the mouse cursor over a connector name and clicking:

Connector	Page
Connector locations	77
Ethernet	79
Host PCI	80
Host peripheral	82
Keyboard	83
Mouse	83
PMC	84
RS-232 port (COM A)	86
SVGA (display monitor interface)	86
USB	86
VMEbus P1	87
VMEbus and interface P2	88
Reset switch	89

Connector locations

Figure C-1 shows the locations of the connectors on the main EPC-1316 board.

For information about installing peripherals and jumper settings, see *Chapter 2, Configuration and installation.*

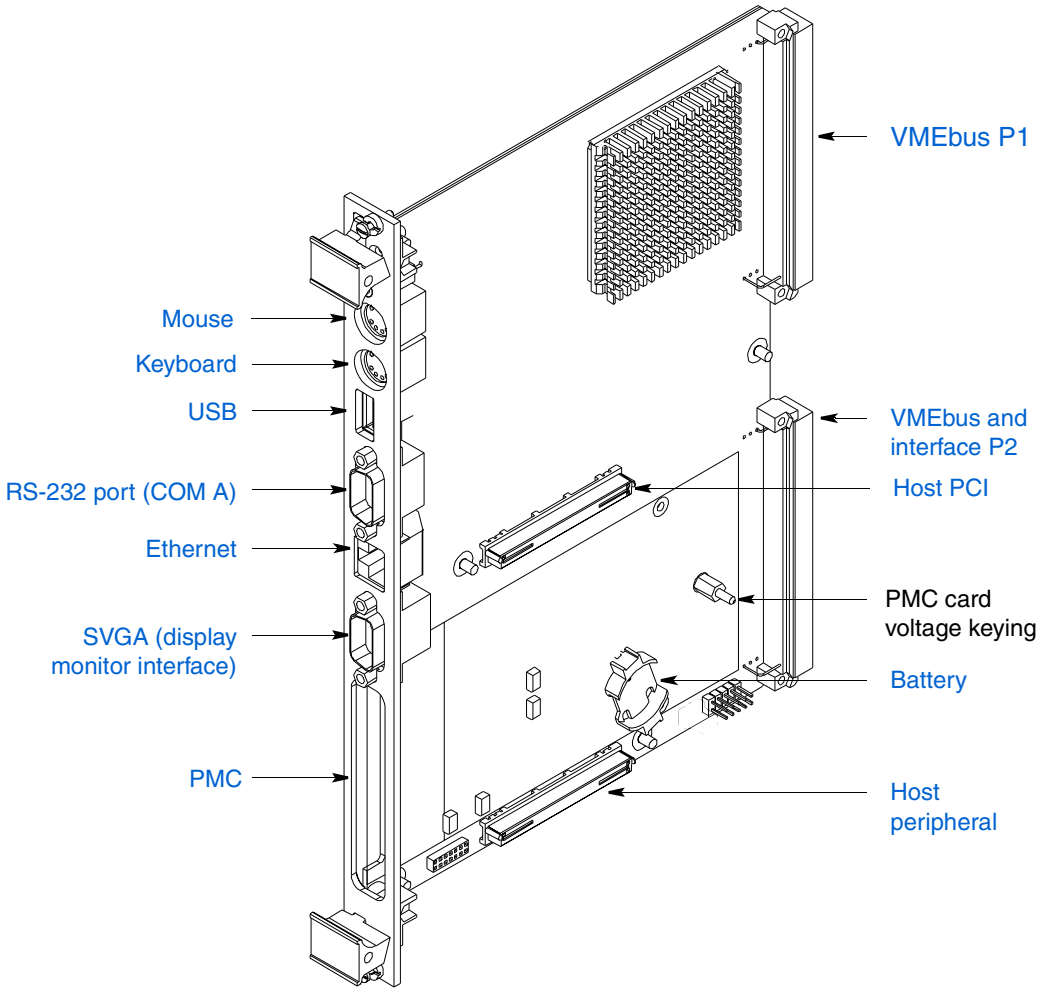


Figure C-1. EPC-1316 assembly: main board connectors

Ethernet

The DTE RJ-45 phone jack supplies the 100/10BASE-T interface to the Ethernet controller.

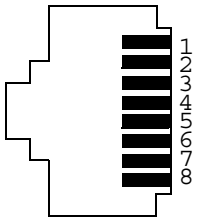


Table C-1. RJ45 phone jack pin-out

Pin	Signal	Pin	Signal
1	Transmit+	5	Center tap TX
2	Transmit–	6	Receive–
3	Receive+	7	Center tap RX
4	Center tap TX	8	Center tap RX

The Ethernet connector also includes these LEDs:

LED	Color	Description
LINK	Green	Indicates the Ethernet link status. This is the LED located nearest the VGA connector. When on, the adapter has a valid link on its network connection and is ready for normal operation (10BASE–T link or 100BASE–TX link). When off, the adapter did not find a valid 10/100BASE-TX link on its network connection; transmit and receive are not possible.
ACT	Green	Indicates Ethernet activity. This is the LED located nearest the COM port. The LED indicates the transmit or receive activity for the 10BASE–T or 100BASE–TX network connections. When on, a packet is being transmitted or received. When off, there is no transmission activity.

Host PCI

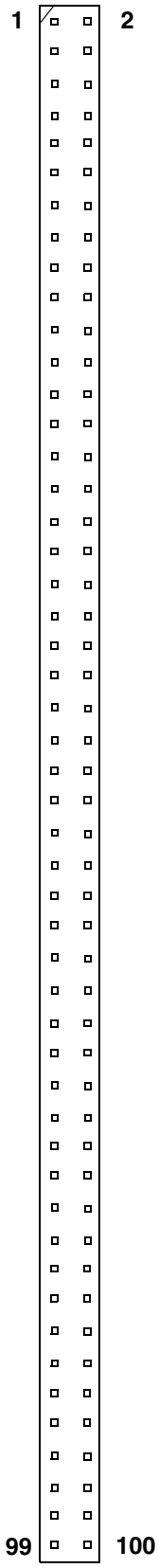


Table C-2. Host PCI connector

Pin	Signal	Pin	Signal
1	PCI:~IRQC	2	PCI:~IRQB
3	PCI:~IRQA	4	PCI:~IRQD
5		6	–12V
7	PCI:CLKSCSI	8	PCI:CLKBRDG
9	NC	10	NC
11	PCI:~GNT2	12	PCI:~REQ3
13	PCI:AD0	14	PCI:AD1
15	PCI:AD2	16	PCI:AD3
17	PCI:AD4	18	PCI:AD5
19	PCI:AD6	20	PCI:AD7
21	PCI:AD8	22	PCI:AD9
23	PCI:AD10	24	PCI:AD11
25	PCI:AD12	26	PCI:AD13
27	PCI:AD14	28	PCI:AD15
29	PCI:AD16	30	PCI:AD17
31	PCI:AD18	32	PCI:AD19
33	PCI:AD20	34	PCI:AD21
35	PCI:AD22	36	PCI:AD23
37	PCI:AD24	38	PCI:AD25
39	PCI:AD26	40	PCI:AD27
41	PCI:AD28	42	PCI:AD29
43	PCI:AD30	44	PCI:AD31
45	NC	46	NC
47	PCI:~FRAME	48	PCI:~STOP
49	PCI:~IRDY	50	PCI:~DEVSEL
51	PCI:~LOCK	52	PCI:~SERR
53	PCI:~TRDY	54	PCI:~PERR
55	PCI:C/~BE0	56	PCI:~C/~BE1
57	PCI:~C/~BE2	58	PCI:~C/~BE3
59	PCI:JPAR	60	PCI:~RST
61	NC	62	NC
63	3.3V	64	3.3V
65	3.3V	66	3.3V
67	3.3V	68	3.3V
69	Reserved	70	Reserved
71	Reserved	72	Reserved
73	~RXD2	74	~R12
75	~DCD2	76	~DSR2
77	~RTS2	78	~TXD2

Table C-3. Host PCI connector power pins

Pin	Signal	Pin	Signal
79	~DTR2	80	~CTS2
81	GND	82	GND
83	GND	84	GND
85	NC	86	GND
87	GND	88	GND
89	GND	90	NC
91	GND	92	GND
93	GND	94	GND
95	NC	96	+5V
97	+5V	98	+5V
99	+5V		

Host peripheral

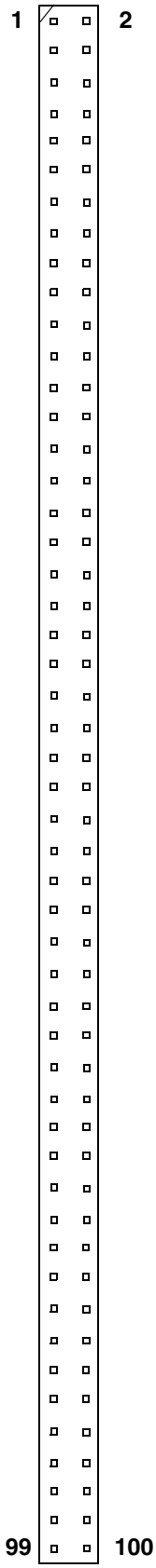


Table C-4. Host peripheral connector

Pin	Signal	Pin	Signal
1	FD:~DENSEL	2	FD:~WRDATA
3	FD:~INDEX	4	FD:~WE
5	+12V	6	–12V
7	FD:~DS1	8	FD:~TRK0
9	FD:~ME1	10	FD:~WP
11	FD:~DIR	12	FD:~RDDATA
13	FD:~STEP	14	FD:~HDSEL
15	FD:~DRATE0	16	FD:~DSKCHG
17	+5 Volts	18	+5 Volts
19	+5 Volts	20	+5 Volts
21	LPT:~STB	22	NC
23	LPT:D0	24	LPT:D4
25	LPT:D1	26	LPT:D5
27	LPT:D2	28	LPT:D6
29	LPT:D3	30	LPT:D7
31	LPT:~ACK	32	LPT:~AF (Auto Feed)
33	LPT:BUSY	34	LPT:~ERR
35	LPT:PE	36	LPT:~INIT
37	LPT:SELECT	38	LPT:~SELIN
39	+5 Volts	40	+5 Volts
41	+5 Volts	42	+5 Volts
43	PIDE:D0	44	PIDE:D8
45	PIDE:D1	46	PIDE:D9
47	PIDE:D2	48	PIDE:D10
49	PIDE:D3	50	PIDE:D11
51	PIDE:D4	52	PIDE:D12
53	PIDE:D5	54	PIDE:D13
55	PIDE:D6	56	PIDE:D14
57	PIDE:D7	58	PIDE:D15
59	Signal GND	60	+5 Volts
61	PIDE:DRQ	62	+5 Volts
63	PIDE:~IOW	64	PIDE:~RST
65	PIDE:~IOR	66	FD:~DS0
67	PIDE:IORDY	68	FD:me0
69	PIDE:~DAK	70	Signal GND
71	AT.IRQ14	72	NC
73	PIDE:SA1	74	NC
75	PIDE:SA0	76	PIDE:SA2
77	PIDE:~CS0	78	PIDE:~CS1
79	PIDE:~ACT	80	NC

Table C-5. Host peripheral connector power pins

Pin	Signal	Pin	Signal
81	GND	82	GND
83	GND	84	GND
85	NC	86	GND
87	GND	88	GND
89	GND	90	NC
91	GND	92	GND
93	GND	94	GND
95	NC	96	+5V
97	+5V	98	+5V
99	+5V		

Keyboard

The keyboard connector is a 6-pin mini-DIN defined as:

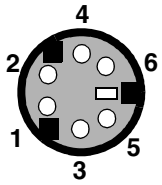


Table C-6. Keyboard pin-out

Pin	Signal	Pin	Signal
1	Data	4	+5V
2	Not used	5	Clock
3	Ground	6	Not used

Mouse

The connector is a PS/2 6-pin mini-DIN defined as:

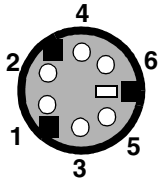


Table C-7. Mouse pin-out

Pin	Signal	Pin	Signal
1	Data	4	+5V
2	Not used	5	Clock
3	Ground	6	Not used

PMC

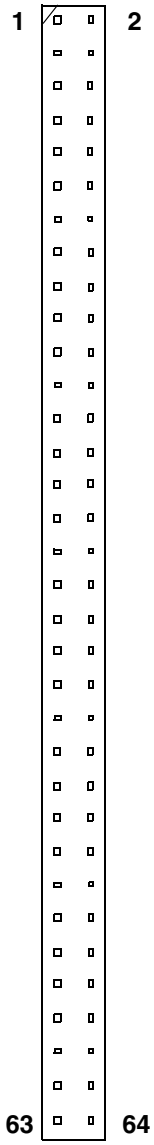


Table C-8. PMC 1 connector pin-out

Pin	Signal	Pin	Signal
1	TCK	2	–12V
3	GND	4	~INTC
5	~INTD	6	~INTA
7	~BUSMODE1	8	+5V
9	~INTB	10	PCI-RSVD
11	GND	12	PCI-RSVD
13	CLK	14	GND
15	GND	16	~GNT
17	~REQ	18	+5v
19	V I/O	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	~C/BE3
27	AD22	28	AD21
29	AD19	30	+5v
31	V I/O	32	AD17
33	~FRAME	34	GND
35	GND	36	~IDY
37	~DEVSEL	38	+5V
39	GND	40	~LOCK
41	~SDONE	42	~SBO
43	PAR	44	GND
45	V I/O	46	AD15
47	AD12	48	AD11
49	AD9	50	+5V
51	GND	52	~C/BE0
53	AD6	54	AD5
55	AD4	56	GND
57	V I/O	58	AD3
59	AD2	60	AD1
61	AD0	62	+5V
63	GND	64	~REQ64

- "~" denotes the signal is active when in the low-logic state.
- PMC-RSVD are no-connect pins reserved for future use.
- VI/O signals are connected to +5V in accordance with the 5V PCI bus signaling requirements.

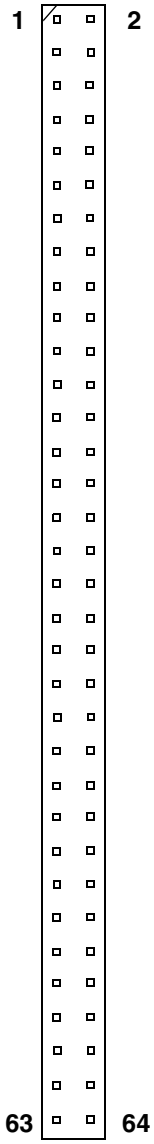


Table C-9. PMC 2 connector pin-out

Pin	Signal	Pin	Signal
1	+12v	2	~TRST
3	TMS	4	TDO
5	TDI	6	GND
7	GND	8	PCI-RSVD
9	PCI-RSVD	10	PCI-RSVD
11	~BUSMODE2	12	+3.3V
13	~RST	14	~BUSMODE3
15	+3.3V	16	~BUSMODE4
17	PCI-RSVD	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3V
25	IDSEL[1]	26	AD23
27	+3.3V	28	AD20
29	AD18	30	GND
31	AD16	32	~C/BE2
33	GND	34	PMC-RSVD
35	~TRDY	36	+3.3V
37	GND	38	~STOP
39	~PERR	40	GND
41	+3.3V	42	~SERR
43	~C/BE1	44	GND
45	AD14	46	AD13
47	GND	48	AD10
49	AD8	50	+3.3V
51	AD7	52	PMC-RSVD
53	+3.3V	54	PMC=RSVD
55	PMC-RSVD	56	GND
57	PMC-RSVD	58	PMC-RSVD
59	GND	60	PMC-RSVD
61	~ACK64	62	+3.3V
63	GND	64	PMC-RSVD

- "~" denotes the signal is active when in the low-logic state.
- PMC-RSVD are no-connect pins reserved for future use.

[1] IDSEL is connected to AD14 (Device 3).

RS-232 port (COM A)

The RS-232 serial port is a male DB-9 DTE.

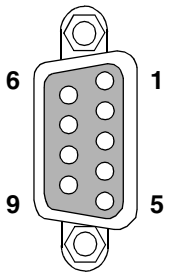


Table C-10. DB-9 pin-out

Pin	Signal	Pin	Signal
1	Data carrier detect (IN)	6	Data set ready (IN)
2	Receive data (IN)	7	Request to send (OUT)
3	Transmit data (OUT)	8	Clear to send (IN)
4	Data terminal ready (OUT)	9	Ring indicator (IN)
5	Signal ground		

SVGA (display monitor interface)

The SVGA DB-15 monitor connector, located on the front panel, is defined as follows:

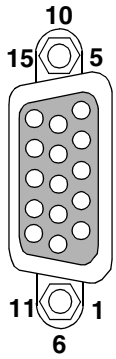


Table C-11. DB-15 pin-out

Pin	Signal	Pin	Signal
1	Red (analog)	9	NC
2	Green (analog)	10	Ground
3	Blue (analog)	11	NC
4	NC	12	NC
5	Ground	13	Horizontal synchronization
6	Analog ground	14	Vertical syncchronization
7	Analog ground	15	NC
8	Analog ground		

USB

The USB (Universal Serial Bus) connector is a 4-pin connector defined as follows:

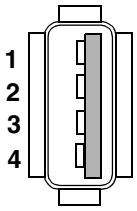


Table C-12. USB connector

Pin	Signal
Mechanical solder lug	Shield ground
1	+5 Volts (1Amp fused)
2	DATA–
3	DATA+
4	Signal ground
Mechanical solder lug	Shield ground

VMEbus P1

This product includes a standard VMEbus P1 connector. It does not access the P1 pins +5VSTDBY, SERCLK, and SERDAT.

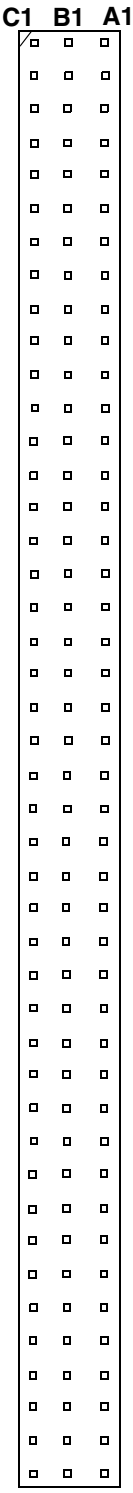


Table C-13. VMEbus P1 connector pin-out

Pin	Signal	Pin	Signal	Pin	Signal
A1	D0	B1	~BBSY	C1	D8
A2	D1	B2	~BCLR	C2	D9
A3	D2	B3	~ACFAIL	C3	D10
A4	D3	B4	~BG0IN	C4	D11
A5	D4	B5	~BG0OUT	C5	D12
A6	D5	B6	~BG1IN	C6	D13
A7	D6	B7	~BG1OUT	C7	D14
A8	D7	B8	~BG2IN	C8	D15
A9	GND	B9	~BG2OUT	C9	GND
A10	SYSCLK	B10	~BG3IN	C10	~SYSFAIL
A11	GND	B11	~BG3OUT	C11	~BERR
A12	~DS1	B12	~BR0	C12	~SYSRESET
A13	~DS0	B13	~BR1	C13	~LWORD
A14	~WRITE	B14	~BR2	C14	AM5
A15	GND	B15	~BR3	C15	A23
A16	~DTACK	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	~AS	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	~IACK	B20	GND	C20	A18
A21	~IACKIN	B21	SERCLK	C21	A17
A22	~IACKOUT	B22	~SERDAT	C22	A16
A23	AM4	B23	GND	C23	A15
A24	A7	B24	~IRQ7	C24	A14
A25	A6	B25	~IRQ6	C25	A13
A26	A5	B26	~IRQ5	C26	A12
A27	A4	B27	~IRQ4	C27	A11
A28	A3	B28	~IRQ3	C28	A10
A29	A2	B29	~IRQ2	C29	A9
A30	A1	B30	~IRQ1	C30	A8
A31	–12V	B31	+5 Volts STDBY	C31	+12V
A32	+5 Volts	B32	+5 Volts	C32	+5 Volts

VMEbus and interface P2

This product includes a standard VMEbus P2 connector which uses the center row for VME and the outer rows for board-specific interface connections. It contains the standard VME signals, IDE signals, floppy signals, parallel port signals and a reset control signal, along with power supply connections to the VME backplane. This connector is used to increase the address and data width of the VME bus to 32 bits of data and 32 bits of address.

The floppy and parallel signals are duplicated on the carrier I/O card front panel. The reset switch signal is wire-ORed with the front panel switch.

Table C-14. VMEbus P2 connector pin-out

Interface	Pin	Signal	Pin	Signal	Pin	Signal
IDE	A1	IDE:D0	B1	VCC	C1	IDE:~RST
	A2	IDE:D1	B2	GND	C2	IDE:D8
	A3	IDE:D2	B3	RESERVED	C3	IDE:D9
	A4	IDE:D3	B4	A24	C4	IDE:D10
	A5	IDE:D4	B5	A25	C5	IDE:D11
	A6	IDE:D5	B6	A26	C6	IDE:D12
	A7	IDE:D6	B7	A27	C7	IDE:D13
	A8	IDE:D7	B8	A28	C8	IDE:D14
	A9	IDE:DRQ	B9	A29	C9	IDE:D15
	A10	IDE:~IOW	B10	A30	C10	NC
	A11	IDE:~IOR	B11	A31	C11	IDE:~CS0
	A12	IDE:CHRDY	B12	GND	C12	IDE:~CS1
	A13	IDE:~DACK	B13	VCC	C13	IDE:~ACT
	A14	IDE:IRQ	B14	D16	C14	IDE:SA0
	A15	IDE:SA1	B15	D17	C15	IDE:SA2
Parallel	A16	LPT:~STB	B16	D18	C16	LPT:~AF
	A17	LPT:D0	B17	D19	C17	LPT:~ERR
	A18	LPT:D1	B18	D20	C18	LPT:~INIT
	A19	LPT:D2	B19	D21	C19	LPT:~SELIN
	A20	LPT:D3	B20	D22	C20	LPT:~ACK
	A21	LPT:D4	B21	D23	C21	LPT:BUSY
	A22	LPT:D5	B22	GND	C22	LPT:PE
	A23	LPT:D6	B23	D24	C23	LPT:SEL
	A24	LPT:D7	B24	D25	C24	FD:DRATE0
Floppy	A25	FD:~DENSEL	B25	D26	C25	FD:~INDEX
	A26	FD:~ME0	B26	D27	C26	FD:~DS1
	A27	FD:~DS0	B27	D28	C27	FD:~ME1
	A28	FD:~DIR	B28	D29	C28	FD:~STEP
	A29	FD:~WRDATA	B29	D30	C29	FD:~WE
	A30	FD:~TRK0	B30	D31	C30	FD:~WP
	A31	FD:~RDDATA	B31	GND	C31	FD:~HDSEL
Reset	A32	~SWRES	B32	VCC	C32	FD:~DSKCHG

Reset switch

The front panel includes a push-button reset switch. An external chassis mounted reset switch can be connected to the P2 connector via the ~SWRES signal.

D Registers

Registers specific to the EPC-1316

Registers in the I/O space that are specific to the EPC-1316 are defined below. Only registers 814Ch–814Fh are "dual-ported" to both the PC and VMEbus. The PC port uses the addresses shown below. The VME addresses for the registers 814Ch–814Fh are described later in this appendix.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	I/O port
Message High Register	MH[7..0]								814Ch
Message High Register	MH[15..8]								814Dh
Message Low Register	ML[7..0]								814Eh
Message Low Register	ML[15..8]								814Fh
Control Register	N/A	1	1	SLOT1	RONR	WDTR	WDTV		8150h
ULA	ULA[7..0]								8151h
VME Event Register	1	1	1	1	~IAKS	~MSGE	~SIGE	~WDTE	8152h
VME Event Enable Register	LRRY	LWRY	0	0	IAKSIE	MSGIE	SIGIE	WDTIE	8153h
Status/Control Register	SRIE	1	SYSC	1	RDY	PASS	NOSF	RSTP	8154h
Status/Control Register	SIE	N/A	SYSR	1	1	1	1	1	8155h
Model Register	MODEL								8156h
Signal FIFO Low	SRFL								8158h
Signal FIFO High	SRFH								8159h
Response Register	LOCK	RRIE	ABMH	SIG	MLK	WRC	FSIG	LSIG	815Ah
Response Register	0	1	DOR	DIR	ERR	RRY	WRY	1	815Bh
IRQ Register	0	0	0	0	0	IRQ[2..0]			8161h
IACK Latch 1 Low	IACK1[7..0]								8162h
IACK Latch 1 High	IACK1[15..8]								8163h
IACK Latch 2 Low	IACK2[7..0]								8164h
IACK Latch 2 High	IACK2[15..8]								8165h
IACK Latch 3 Low	IACK3[7..0]								8166h
IACK Latch 3 High	IACK3[15..8]								8167h
IACK Latch 4 Low	IACK4[7..0]								8168h
IACK Latch 4 High	IACK4[15..8]								8169h
IACK Latch 5 Low	IACK5[7..0]								816Ah
IACK Latch 5 High	IACK5[15..8]								816Bh
IACK Latch 6 Low	IACK6[7..0]								816Ch
IACK Latch 6 High	IACK6[15..8]								816Dh
IACK Latch 7 Low	IACK7[7..0]								816Eh
IACK Latch 7 High	IACK7[15..8]								816Fh

VXI Register Offsets—see *VXI register base address decoding* on page 100 for base address determination.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	I/O port
ID/ULA register	8Fh								0h
ID/ULA register	ECh								1h
Device type register	0001 000S								2h
Device type register	MM								3h
Status/control register	SRIE	1	SYSC	1	RDY	PASS	NOSF	RSTP	4h
Status/control register	0	N/A	SYSR	1	1	1	1	1	5h
Protocol low register	1Fh								8h
Protocol high register	FFh								9h
Response register	0	1	DOR	DIR	ERR	WRC	WRY	1	Ah
Response register	LOCK	RRIE	ABMH	SIG	MLK	RRY	FSIG	LSIG	Bh
Message high register	MH[15..8]								Ch
Message high register	MH[7..0]								Dh
Message low register	ML[15..8]								Eh
Message low register	ML[7..0]								Fh

Register details

Message registers (814Ch–814Fh)

High	MH[7..0]
High	MH[15..8]
Low	ML[7..0]
Low	ML[15..8]

This is the PC-port side of the VXI message registers.

Each of the 16-bit Message registers is actually two registers, an inbound register and an outbound register. There are actually four 16-bit locations:

- Message high in
- Message high out
- Message low in
- Message low out

Writing from the PC port writes to the outbound register. Reading from the PC port reads the inbound register. Writing from VME writes to the inbound register. Reading from VME reads the outbound register. The inbound register is situated on the ISA bus for reads and the outbound register is situated on the VME bus for reads.

ABMH in the Response register, described below, is cleared when the low byte of Message High register is written from VME. It serves as a location monitor for determining whether a message is 16 or 32 bits in length. Access from the PC port has no effect on ABMH.

When the low byte of Message Low is read from VME, RRY in the Response register is cleared. When the low byte of Message Low is written from VME, WRY in the Response register is cleared. Access from PC port has no effect on RRY and WRY.

The low byte of Message-Low-out register is driven onto the VMEbus D[15:8] during an IACK response cycle. VMEbus D[7:0] is driven from the ULA register.

Control register (8150)

1	1	1	SLOT1	RONR	WDTR	WDTV

Only WDTR is cleared by a warm reset. All bits are cleared by a reset.

SLOT1 Read only bit that indicates that state of the Slot-1 detect. A ‘1’ indicates SLOT1 controller.

RONR Bus release mode. If set, the bus release mode is RONR (request on no request); otherwise it is controlled by the bus request bits in the Universe chip.

WDTR Watchdog timer reset enable. A read of the this register should be performed before enabling the watchdog timer reset to clear the watchdog counter to zero so that a PC reset does not occur immediately after enabling the watchdog timer. Possible values include:

1 Expiration of the watchdog timer causes a reset.

0 Only the WDT event is signaled.

WDTV Watchdog timer value. This field produces the following timeout values:

00 (disables events from the watchdog timer)

01–8.2s

10–128ms

11–1.02s

A read of the this register also has a side effect of resetting the watchdog timer. Therefore, if using the watchdog timer, it is required to read this register within the defined period of the timer to prevent generating an interrupt.

ULA (8151h)

ULA[7..0]

The ULA register is an 8-bit value that represents the Unique Logical Address of the VXI registers. This register is driven onto the VME bus D[7:0] during an IACK response cycle. VME D[15:8] is driven from the lower 8 bits of the Message Low register.

VME event register (8152h)

1	1	1	1	~IAKS	~MSGE	~SIGE	~WDTE

This register defines conditions that may result in an interrupt. If the bit is 0, the condition is present.

~WDTE Watchdog timer expired.

~SIGE Signal FIFO is not empty.

~MSGE If clear, a message interrupt is being signaled. MSGE is cleared if both of bits RRDY and WRDY in the response register are clear.

~IAKS To be determined.

All bits are read-only.

VME event enable register (8153h)

LRRY	LWRY	0	0	IAKSIE	MSGIE	SIGIE	WDTIE

The LRRY and LWRY are used as latching bits which hold the event of a RRY or WRY transition from a high to a low state. Thus if RRY transitions from a high to a low state (indicates a read of the VME message register occurred), then LRRY is set to a one. The same is true for the LWRY in the instance of a write to the message register. These bits can individually be reset to a zero state by writing a one to the respective bit field. Thus to clear LRRY, write a one in the MSB by ORing the current state of the register with the value of 80h. In the case of the LWRY a 40h would be ORed with the current value of the register.

If the MSGE bit is asserted and LRRY or LWRY is set, then an interrupt from the FPGA is signaled to the processor. (For example, AT interrupt 10 is asserted to the processor.)

The IAKSIE bit indicates when an interrupt acknowledge is occurring. It indicates the actual value of the IAKSIE signal line on the VME bus.

These bits are a mask of the interrupt conditions in the event state register. A one denotes that the corresponding event is enabled as an interrupt. If any bit in this register is a one, and the corresponding bit in the event state register is a zero, IRQ10 interrupt is asserted. Software may then examine the interrupt and event state registers to determine the cause. Reset clears this register.

Status/control register (8154h)

SRIE	1	SYSC	1	RDY	PASS	NOSF	RSTP

Status/control register (8155h)

SIE	N/A	SYSR	1	1	1	1	1

These registers adhere to the VXIbus specification and also contains EPC-1316 specific bits. Bits RSTP and NOSF are writable only from the VME port. Bits SRIE, RDY, PASS, SYSR are writable only from the PC Port. All bits are readable from both ports. See the VXI register description for details of each bit definition.

Model register (8156h)

MODEL

This register is a write once register after reset. The BIOS loads this with the model number based on the EPC model. Once written, it is read only as the low 8 bits of the device type register in the VXI register space. Hardware reset enables writing the register again.

Signal FIFO low (8158h)

SRFL

Signal FIFO high (8159h)

SRFH

To spell out the operation of the signal register FIFO, and associated control bits, the operations are explained in algorithmic fashion. SIG, FSIG and LSIG are fields in the Response register.

The signal FIFO (SRFIFO) is a two-element array with indexes. A write to the Protocol register from the VXI bus (see *VXI register details* on page 96) is a write to the signal FIFO, and does the following:

```
if (SIG && (FSIG != LSIG)) { /* FIFO full */
   Assert BERR
}

else {
   if (SIG) LSIG = !LSIG;
   SRFIFO[LSIG] = write data;
   SIG = 1
}
```

A read from SRFL returns the low-order byte of SRFIFO(FSIG). In all cases of accesses to SRFL and SRFH, if SIG = 0 (empty FIFO), the result is an access to SRFIFO (0). A read from SRFH returns the high-order byte of SRFIFO(FSIG), and does the following:

```
if (FSIG == LSIG) { SIG = LSIG = FSIG = 0 }
else FSIG = !FSIG;
```

Response register (815Ah)

LOCK	RRIE	ABMH	SIG	MLK	WRC	FSIG	LSIG

Response register (815Bh)

0	1	DOR	DIR	ERR	RRY	WRY	1

The Response Register is described below, in the Response Register description in *VXI Register Details*.

IRQ register (8161h)

0	0	0	0	0	IRQ[2..0]

This register specifies which VME interrupt is to be asserted. 000 indicates none. 001 means assert IRQ1, 010 means assert IRQ2, 111 means assert IRQ7. The register is cleared at reset or whenever an IACK to the interrupt asserted by this module occurs. Clearing the register de-asserts any interrupt that was asserted.

IACK latches (8162h–816Fh)

High	MH[7..0]
Latch 1 low	IACK1[7..0]
Latch 1 high	IACK1[15..8]
Latch 2 low	IACK2[7..0]
Latch 2 high	IACK2[15..8]
Latch 3 low	IACK3[7..0]
Latch 3 high	IACK3[15..8]
Latch 4 low	IACK4[7..0]
Latch 4 high	IACK4[15..8]
Latch 5 low	IACK5[7..0]
Latch 5 high	IACK5[15..8]
Latch 6 low	IACK6[7..0]
Latch 6 high	IACK6[15..8]
Latch 7 low	IACK7[7..0]
Latch 7 high	IACK7[15..8]

All bits are cleared by a PCI reset.

IACK Latch is a 16-bit value latched from the VMEbus during an IACK cycle generated by this VME module. This value allows one to claim the full 16-bit data value of an IACK cycle. This is useful because, for some reason, the Universe chip strips off the upper 8 bits and flips bit 0. Each IACK Latch register corresponds to a different VME interrupt.

VXI register details

The addresses shown are offsets relative to a base address. See *VXI register base address decoding* later in this chapter for the method for determining the base address.

If a bit is shown as 0 or 1, the bit is a ROM bit, and writing to it has no effect. Except as otherwise noted below, all registers and bit values can be read and written.

ID/ULA register (offset 0h)

8Fh

ID/ULA register (offset 1h)

ECh

This register adheres to the VXIbus specification. It defines EPC-1316 as a message-based device and the manufacturer as RadiSys. When read, the ID is returned. When written, the lower 8 bits define the unique logical address (ULA). The upper 8 bits are ignored. The ULA is not valid as an addressing mechanism until the register is written the first time. Until then, one must use the MODID address mechanism (For example, ULA of FFh with MODID asserted) to address the VXI registers.

Device type register (offset 2h)

0001 000S

Device type register (offset 3h)

MM

These registers adhere to the VXIbus specification. The value defines EPC-1316 as having a model code of 1010h if it is a slot 0 controller and 1110h if it is not a slot 0 controller.

Status/control register (offset 4h)

0	N/A	SYSR	1	1	1	1	1

Status/control register (offset 5h)

SRIE	1	SYSC	1	RDY	PASS	NOSF	RSTP

These registers adhere to the VXIbus specification and also contains EPC-1316 specific bits. Bits RSTP and NOSF are writable only from the VME port. Bits SRIE, RDY, PASS, SYSR are writable only from the PC Port. All bits are readable from both ports.

SRIE — SYSRESET input enable. If set, assertion of VME SYSRESET generates a reset of the EPC-1316. One use of this bit is having EPC-1316 software reset other VME devices (via bit SYSR) without resetting EPC-1316.

SYSC — SYSCLK status bit. All writes to this register have the effect of clearing this bit. The bit is then set if four rising edges of the VXI SYSCLK signal are detected. This bit is intended to be used to detect that SYSCLK is being generated on the backplane.

RDY — This is a RAM bit defined by the VXI specification. In a VXIbus software environment, if RDY=1 and PASS=1, EPC-1316 is ready to accept VXI-defined messages.

PASS — If set (1), EPC-1316 has completed its self-test successfully. If this bit is cleared (0), indicating that the self-test failed.

NOSF — SYSFAIL inhibit. If set (1), EPC-1316 does not assert the VMEbus SYSFAIL line due to the PASS bit being cleared. If the PASS bit is cleared and this bit is cleared (0), then SYSFAIL is asserted. SYSFAIL is also asserted when a Watchdog timeout reset occurs, independent of the setting of this bit. Assertion of SYSFAIL can also be accomplished by application software writing to bit 30 of the Universe VCSR_SET and VCSR_CLR registers.

RSTP — Reset processor. Setting this bit to a 1 resets the EPC-1316.

N/A — Not defined.

SYSR — SYSRESET. EPC-1316 asserts the VME SYSRESET line while this bit is 1. When using this bit, it is the software's responsibility to ensure that the VME-specified minimum assertion time of SYSRESET is met. This function can also be performed by bit 22 of Universe register MISC_CTL.

Protocol low register (offset 8h)

1Fh

Protocol high register (offset 9h)

FFh

A read of these registers reads the ROM constants stored in the protocol register. A write to this register location writes the signal register.

The protocol register (the read value) defines EPC-1316 as being a servant and commander, having a signal register, being a bus master and an interrupter, not providing the shared-memory protocol, and not providing fast handshake mode.

Response register (offset Ah)

0	1	DOR	DIR	ERR	WRC	WRY	1

Response register (offset Bh)

LOCK	RRIE	ABMH	SIG	MLK	RRY	FSIG	LSIG

These registers contain some VXI-defined state bits associated with message handling, and several EPC-1316 dependent bits. These registers are read-only from VME and are read/write from the PC port. Note that some of these bits (ABMH, MLK, RRY and WRY) can be cleared by hardware when access is made to the message registers from the VME port. Software protocols as defined by the VXI specification guarantee that this does not happen at the same time as a write from the PC port to these bits. If software violates this protocol, unpredictable results can occur.

LOCK RAM bit available to software for VXI communication protocols.

RRIE This bit is used to enable RRY interrupt signaling. When clear (reset state), only the deassertion of WRY causes the MSGR interrupt to be asserted. When set, the "OR" of the deasserted RRY, WRY bits is used to assert the interrupt.

ABMH This bit is cleared when the message high register is read or written from the VXIbus. It serves as a location monitor for determining whether a message is 16 or 32 bits in length.

SIG If this bit is 0, the signal FIFO is empty.

MLK This bit is used for synchronization of messages from multiple senders, something not provided for in the VXI specification. If 1, the message register can be locked for the sending of a message. If 0, the message register has been locked. See the discussion of message sending protocol, below.

WRC This bit is a read-only copy of the WRY bit.

FSIG Defined only when SIG=1, in which case FSIG is the number (0 or 1) of the register in the FIFO holding the earliest signal.

LSIG Defined only when SIG=1, in which case LSIG is the number (0 or 1) of the register in the FIFO holding the most recent signal.

DOR RAM bit available to software for VXI communication protocols.

DIR RAM bit available to software for VXI communication protocols.

ERR RAM bit available to software for VXI communication protocols.

RRY Read ready. A 1 denotes that the message registers contain outgoing data to be read by another device. RRY is cleared when the message-low register is read from VME. RRY can only be set by writing to this register from the PC port.

WRY Write ready. If set, the message registers are armed for an incoming message. When a write occurs into the message-low register, WRY is cleared and the MSGR interrupt condition is asserted. Wry can only be set by writing to this register from the PC port.

FSIG and LSIG are not used for programming. They are read-only bits used for tests during manufacturing.

The protocol for sending a message, when there are multiple potential senders, is as follows:

1. Read the Alternate Response register (offset 2A).
2. If both WRY and MLK are 1, then proceed to send the message.
3. If not, repeat reads until both WRY and MLK are 1.
4. For 16-bit messages, write into the Message Low register.
5. For 32-bit messages, write first into Message High register and then into the Message Low register.

The bits RRY, WRY, ABMH, and MLK in the Response register are altered by hardware-detected conditions. A read from the Message Low clears RRY. A write into all or the lower 8 bits of the Message Low register clears WRY. A read from the VME bus port of the Alternate Response register clears MLK if WRY is set. A read or write to all or the lower 8 bits of the Message High register clears ABMH. A read from the Alternate Response register also returns the value in the Response register. Note that the Alternate Response register is accessed at offset 0x2A from the VME A16 base address of these registers.

LOCK, RRIE, MLK, ABMH, DIR, DOR, ERR can be set or cleared by using a write to the response register. RRY and WRY may only set via a write to the Response register. For these two bits, a 0 written into the respective bit position does not change the value of the register bit. A 1 written into the respective bit position sets the value of the register bit to 1.

Supporting software on the controller must be aware of how to set the bits initially. Valid states include:

RRY	WRY	MLK	State
X	1	1	Write ready (awaiting incoming msg)
X	1	0	Write ready, locked by a sender
1	X	X	Read ready (outgoing data present)
0	0	X	Not ready for write or read

Message high register (offset Ch)

MH[15..8]

Message high register (offset Dh)

MH[7..0]

Message low register (offset Eh

MH[15..8]

Message low register (offset Fh)

ML[7..0]

See the description above for the operation of these registers.

VXI register base address decoding

To determine the VXI Register Base Address:

1. Read ULA as the lower 8 bits at 8151h. (`xxxx xxxx aaaa aaaa`).
2. Form base address as:

   `11aa aaaa aa00 0000`

   where `aaaa aaaa` are the lower 8 bits at 8151h.

   The result is the binary representation of the VXI Register Base Address.

   Thus the lowest possible base address is C000h (1100 0000 0000 0000) and the highest possible base address is FFC0h (1111 1111 1100 0000). Note that the range consists of base addresses separated by 40h.
3. Configure a VMEbus Target Image with A16 address space and add to the base address from step 2.

   For example, if a VMEbus Target Image is configured from address 800000000h, then the VXI registers for ULA 2 can be accessed by a memory cycle starting ad address 8000C080h.

   Another view:

   `Base_addr = A16 Target Image Base Address + (C000h + (ULA * 40h))`

E Error messages and diagnosis

Boot failures

The System BIOS halts and attempts to display an error message on the VGA monitor when it encounters the following error conditions:

Error	Possible causes
Fixed disk error	No drive connected
	Configured for 0 cylinders
	Controller reset failed
	Drive not ready
	Track 0 seek timed out
	Drive initialization failed
	Drive recalibration failed
	Last track seek failed
Video error	Color/Mono switch not set correctly
Timer error	System timer (0) failed
Diskette error	Floppy type does not match setup
I/O chip error	I/O conflicts exist for serial and parallel ports, floppy, hard disk (any or all)
Other errors	IRQ conflict, unsupported COM port configuration, keyboard locked

Troubleshooting

This section deals with problems that you may encounter that do not provide an error message.

Table E-1. Troubleshooting error messages

Symptoms	Possible cause(s)	Solution
System appears to boot but no video	Monitor or cable problem (with or without onboard video).	Verify that the cable pins are not bent and the cable is fully seated in the video adapter. If necessary, try the monitor on another system to verify that the monitor is good.
System fails at power-up—does not run power-on self-test.	The system is not getting power.	Check the backplane and verify that +5V power is good.
	SODIMM memory module missing or loose.	Check that the SODIMMs are still present and connected. Remove and re-seat SODIMM modules in sockets.
	Hardware failure.	This cannot be diagnosed in the field. Call RadiSys Support.
Serial port(s) do not work.	Bad power.	Verify that backplane +12V and –12V are good.
	Interrupt conflicts	Verify that no other card in the EPC-1316 subsystem is using IRQ3 or IRQ4.
	Port hardware failure.	Call RadiSys Support.
System hangs during boot process	VMEbus has no Slot-1 controller providing bus timeout.	You are probably loading an expanded memory manager (for example, EMM386.EXE) in your CONFIG.SYS file. This can cause the system to hang if there is no Slot-1 controller or the Slot-1 controller is not providing the proper bus timeout.
System does not talk across VMEbus.	The VMEbus backplane may not be jumpered correctly.	See Installing the VMEbus backplane jumper in Chapter 2, Configuration and installation.
	There may be no Slot-1 controller providing bus arbitration.	Determine that the controller is in the leftmost position and that the Slot-1 controller auto-detect is functioning.
	EPC-1316 may have bent pins	Remove the EPC-1316 and verify that no pins are bent. Then reinsert the EPC-1316.
	VMEbus interface failure.	Contact RadiSys Support as described in Where to get more information on page v.

F MSIO Carrier Board

This appendix describes how to configure and use the optional MSIO (Mass Storage I/O) Carrier board. When reading this file online, you can immediately view information about any installation topic by placing the mouse cursor over a connector name and clicking.

Task	Page
Overview	103
Configuration	104
BIOS configuration	107
Organization	108
Connectors	109

Overview

The MSIO Carrier Board connects to the Main board via PCI and peripheral buses, and contains the remaining I/O functions including one RS-232/RS-485 serial port, an IEEE-1284 bi-directional parallel port, and an Ultra SCSI-2 port, EXP-FDM floppy interface, EIDE interface with a 2.5" hard disk drive.

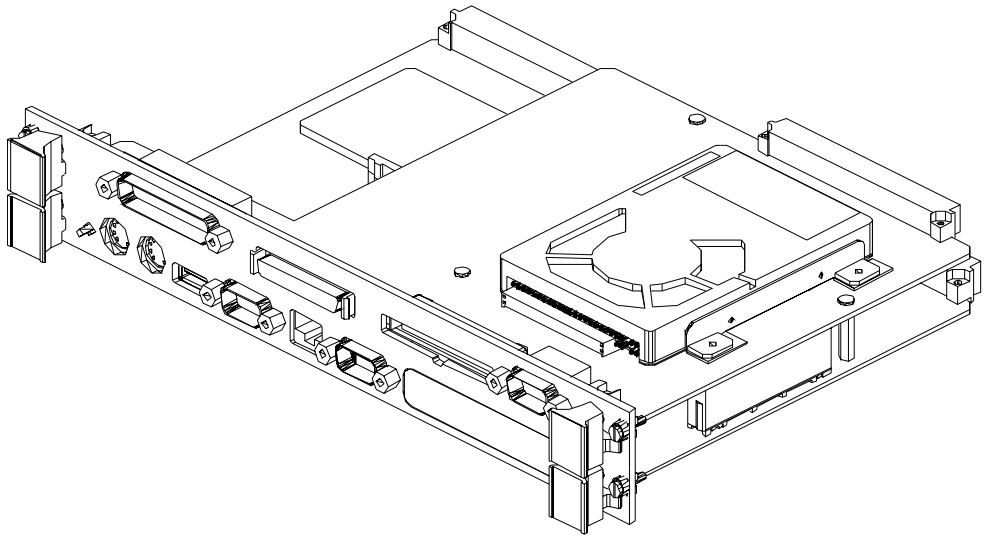


Figure F-1. EPC-1316 with MSIO Carrier Board

Configuration

To configure and install the MSIO Carrier Board, you must complete the steps s shown below.

Task	Page
Setting Jumpers on the MSIO Carrier Board	105
Disconnecting the MSIO Carrier Board	106
Re-assembling the MSIO Carrier Board and the Main board	107

Avoid causing ESD damage:

- Remove modules from their antistatic bags only in a static-free environment.
- Perform the installation process (described later in this chapter) only in a static-free environment.
- During the installation process, ensure that power to your system is off. The EPC-1316 is not designed to be inserted or removed while the chassis is powered up.
- During external cable installation, ensure that the cables are not active. The EPC-1316 is not designed for hot insertion of any interface.

The EPC-1316 modules, like most other electronic devices, are susceptible to electrostatic discharge (ESD) damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

⚠ DANGER

If you plan to connect a floppy drive, you must use a RadiSys EXP-FDM (Floppy Disk Module).

Connecting a standard floppy drive can create a fire hazard and may damage or destroy the EPC-1316 baseboard, MSIO carrier board, EXP-FDM, or cable.

Setting Jumpers on the MSIO Carrier Board

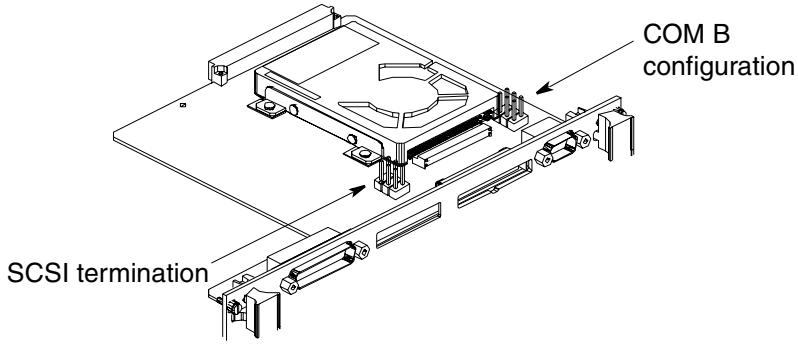
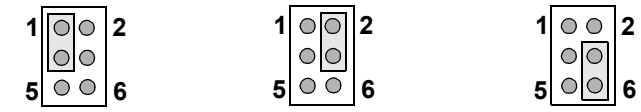


Figure F-2. MSIO Carrier BoardMSIO Carrier Board assembly: jumper locations

Jumper pins are labeled from the point of view of looking at the front of the connector.

COM B configuration

Place the COM B jumpers, located next to the RS-232/RS-485 port (COM B) connector on the MSIO Carrier Board, to set COM B to function as the connector type you desire:



Pins 1 and 3: RS-232

Pins 2 and 4: RS-485 with terminator

Pins 4 and 6: RS-485 without terminator

Figure F-3. COM B jumper settings

When in RS-485 mode, you can configure the interface with or without a 100Ohm terminator across the receive channel data pair.

SCSI termination

When you configure SCSI peripherals to work with the MSIO Carrier Board, you need to consider the placement of the MSIO Carrier Board in the SCSI chain. The MSIO Carrier Board must be terminated if it is the last device in the SCSI chain. You can set the SCSI termination jumpers, located next to the SCSI-2 connector on the MSIO Carrier Board, to determine the following:

Pins 1/3 and 2/4: Enable termination power and terminators

Pins 1/3 and 4/6: Enable termination power and disable terminators

Pins 3/5 and 2/4: Disable termination power and enable terminators

Pins 3/5 and 4/6: Disable termination power and disable terminators

Figure F-4. SCSI jumper settings

Disconnecting the MSIO Carrier Board

If your EPC-1316 includes the MSIO Carrier Board, you must disassemble the board before performing upgrades (such as changing memory or adding options) on the EPC-1316.

To separate the MSIO Carrier Board and the Main board:

1. Remove the EPC-1316 from the VME chassis as described in *Extracting the EPC-1316* on page 13.
2. Remove the screws that attach the MSIO Carrier Board to the Main board (see Figure F-6).
3. Disconnect the boards by pulling apart while keeping them parallel. Continue applying force until the connectors and grips completely disengage.

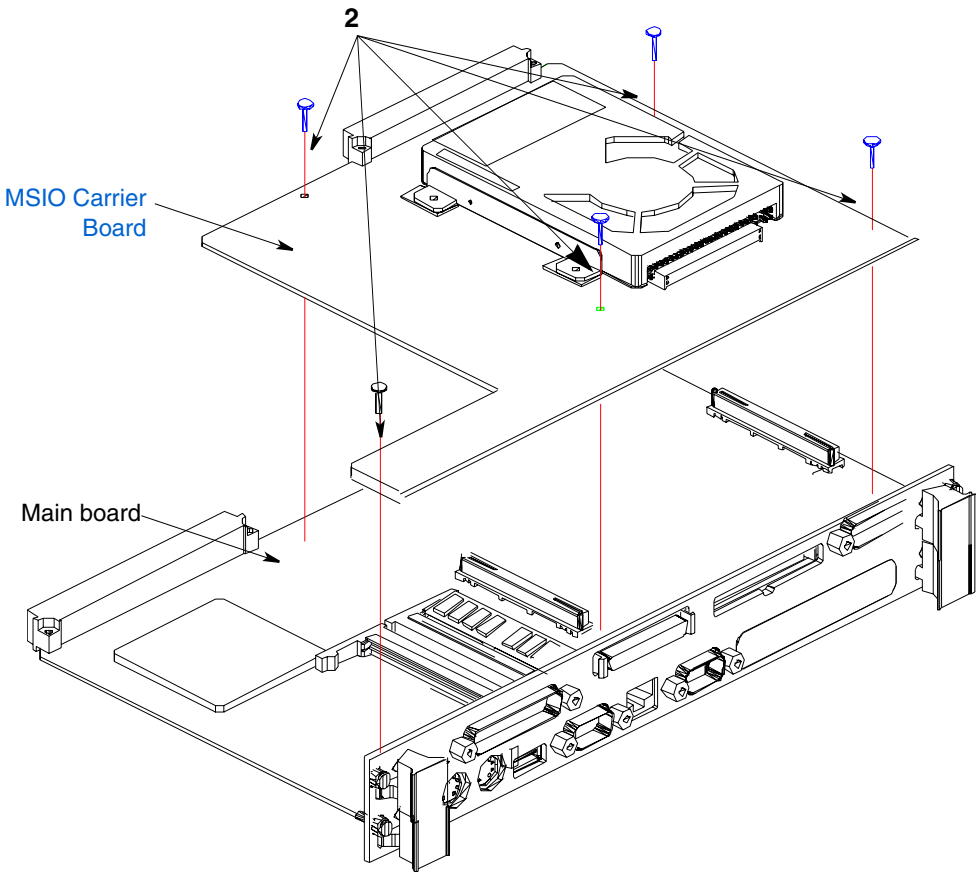


Figure F-5. Disconnecting the optional MSIO Carrier Board

Re-assembling the MSIO Carrier Board and the Main board

1. Remove the EPC-1316 from the VME chassis as described in *Extracting the EPC-1316* on page 12.
2. Connect the main and MSIO Carrier Boards by pushing while keeping them parallel. Continue applying force until the connectors and grips completely engage.
3. Insert the screws that attach the MSIO Carrier Board to the main board (see Figure F-6).

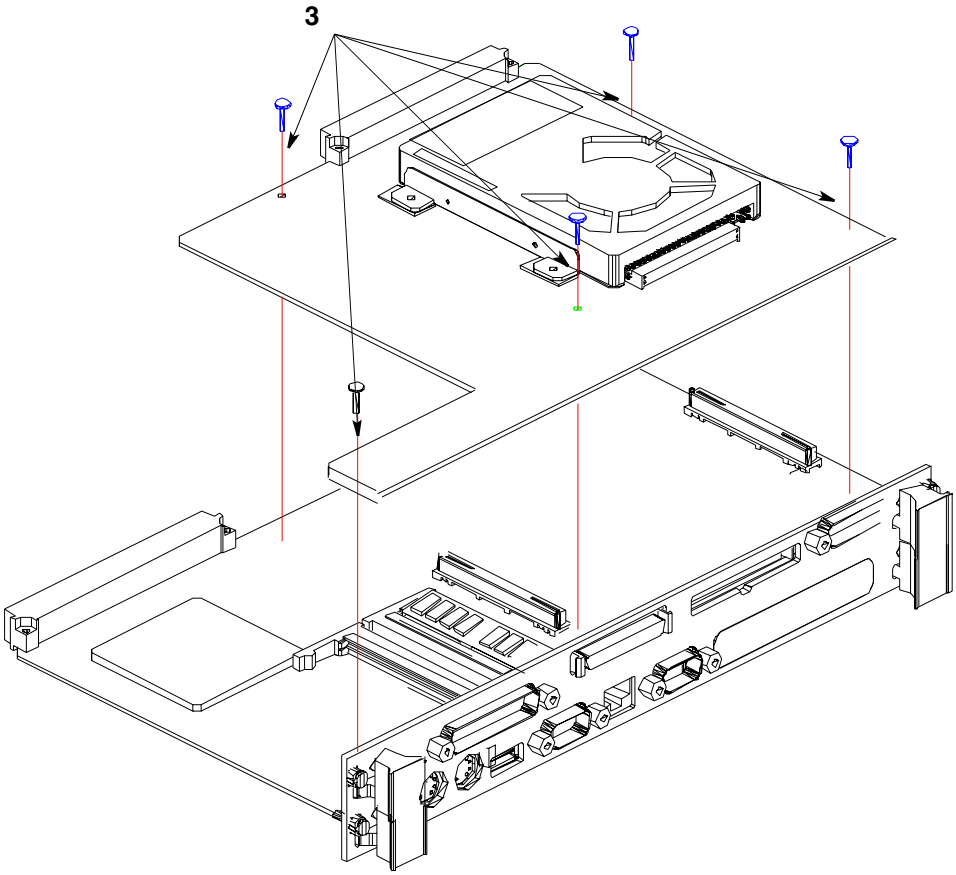


Figure F-6. Attaching the MSIO Carrier Board to the Main board

BIOS configuration

If you plan to connect a floppy drive to the EXP-FDM floppy connector, be sure to:

- Identify the type of floppy disk drive in the appropriate Legacy Diskette field on the Main menu (see page 18).
- Make floppy disk controller is available for use by enabling the Floppy Disk Controller on the *I/O Device Configuration sub-menu* on page 37.

The MSIO Carrier Board has the primary IDE interface. If your EPC-1316 includes the MSIO Carrier Board option, primary IDE is available. To configure the detailed

characteristics of the installed IDE drive, select and configure the appropriate Primary/ Secondary Master/Slave sub-menus (see page 20).

To identify which port the MSIO Carrier Board uses, select and configure the appropriate Serial Port field on the *I/O Device Configuration sub-menu* on page 37.

For detailed information about configuring the BIOS, see *Chapter 3, BIOS configuration*.

Organization

Block diagram

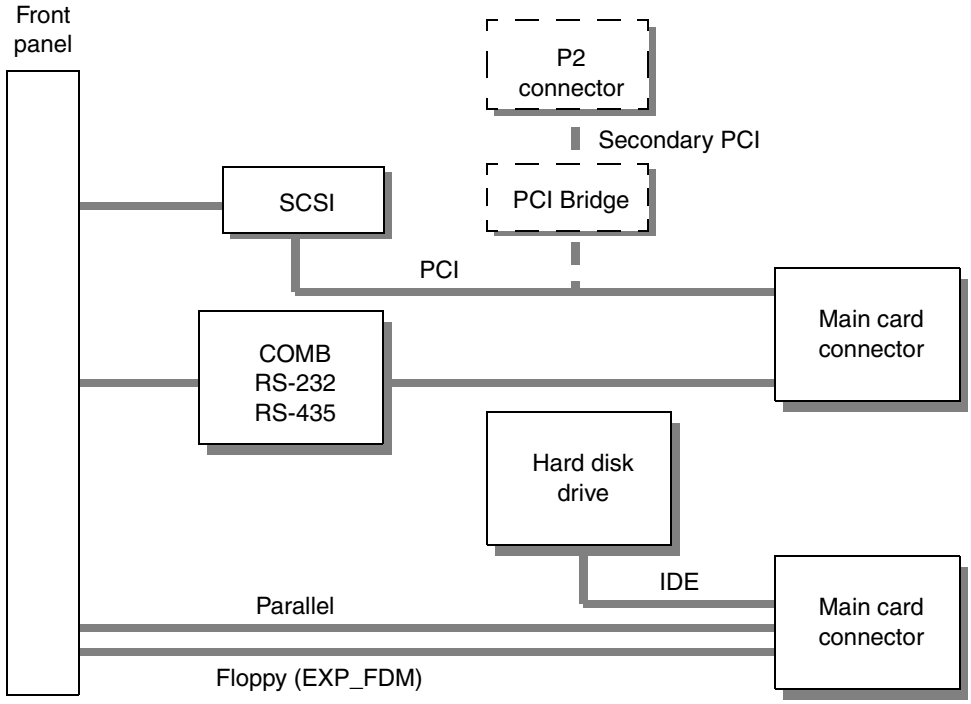


Figure F-7. Block diagram: MSIO Carrier Board

Feature set

SCSI interface

The SCSI interface is located on the MSIO Carrier Board. The SCSI controller, a Symbios 53C860, is a 32-bit device that resides on the PCI bus and provides a single-chip PCI-to-SCSI interface. It supports the SCSI-2 8-bit Fast SCSI interface at 20Mb/second synchronously and 7Mb/second asynchronously. This controller uses PCI interrupt A and DMA channel 3. It is configured through the PCI Configuration Space.

Peripheral ports

The I/O address and IRQ of peripheral ports are determined by the CMOS parameters established by default. This includes one serial port (RS-232/485 (COM B)).

COM B ports

The RS-232 ports are standard PC COM serial ports based on the 16550 architecture. COM B is mapped to I/O address 2F8h–2FFh and uses interrupt IRQ3, and can be configured for either RS-232 or RS-485.

If not needed, COM B can be disabled in the BIOS Setup Integrated Peripherals Sub-Menu to free up the I/O address and interrupt for usage by other expansion products. For more information about configuring COM B, see *COM B configuration* on page 105.

Parallel port

The printer port is a bi-directional IEEE1284-C PC parallel port. The parallel port supports bi-directional communication compatible with the PS/2 definition. It is configured as LPT1, mapped to I/O address 378h–37Fh, and uses interrupt IRQ7. If not needed, LPT1 can be disabled in the BIOS Setup Integrated Peripherals Sub-Menu to free up the I/O address and interrupt for usage by other expansion products. The parallel port is accessible via the front panel or the P2 connector; these are mutually exclusive.

Floppy controller

The National 87309 Super I/O chip, used to implement the serial and parallel port, also implements a standard PC floppy disk port. The device resides on the ISA bus, and is accessed at the standard PC I/O addresses of 3F0h–3F7h. Interrupts are signaled on IRQ6. The floppy disk controller supports up to two floppy interfaces:

- EXP-FDM floppy interface, available on the floppy port as floppy drive A with a 1.44 MByte, 3.5" format.
- Standard PC floppy A/B cabling interface, available on the P2 connector on the EPC-1316 board.

These floppy interfaces are mutually exclusive.

Connectors

The MSIO Carrier Board product includes these connectors and jumpers:

Connector	Page
Connector locations	109
EIDE (primary)	111
EXP-FDM floppy	112
Parallel port	112
RS-232/RS-485 port (COM B)	113
SCSI-2	114

Connector locations

Figure F-8 shows the locations of the connectors on the EPC-1316 MSIO Carrier Board.

For information about installing peripherals and jumper settings, see *Configuration*.

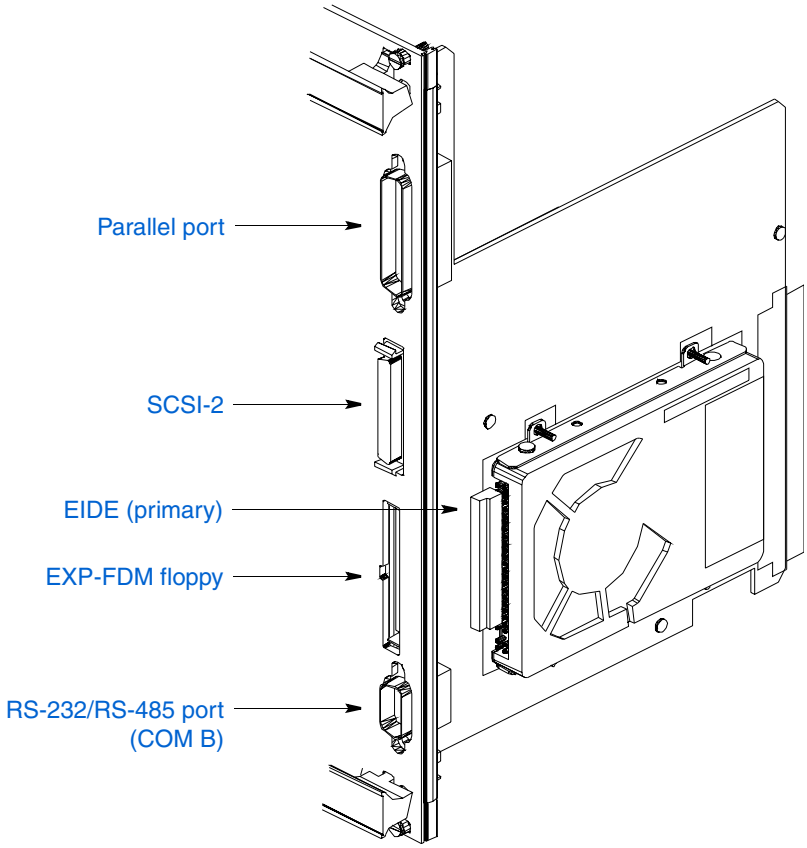


Figure F-8. MSIO Carrier Board: connectors

EIDE (primary)

The Primary EIDE Connector is a male 44-pin right-angle header located on the MSIO Carrier Board. The pins and signals are defined as:

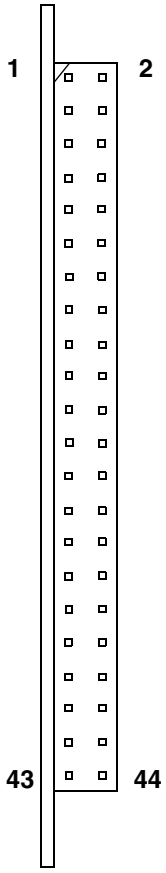


Table F-1. Primary EIDE connector

Pin	Signal	Pin	Signal
1	~RST	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	N.C.
21	DRQ	22	GND
23	~IOW	24	GND
25	~IOR	26	GND
27	IORDY	28	PPU
29	~DAK	30	GND
31	IRQ	32	N.C.
33	A1	34	N.C.
35	A0	36	A2
37	~CS0	38	~CS1
39	ACT	40	GND
41	+5 Volts	42	+5 Volts
43	GND	44	GND

EXP-FDM floppy

The Floppy disk drive connector is a male 34-pin header located on the front panel of the MSIO Carrier Board. The pins and signals are defined as:

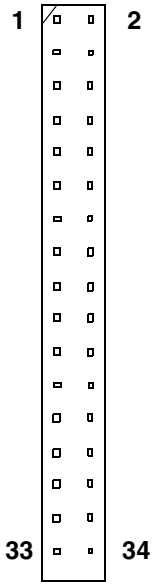


Table F-2. EXP-FDM floppy connector

Pin	Signal	Pin	Signal
1	GND	2	DENSEL
3	N.C.	4	N.C.
5	N.C.	6	RATE0
7	+5 Volts	8	INDEX
9	+5 Volts	10	N.C.
11	+5 Volts	12	DS1
13	GND	14	N.C.
15	GND	16	MTR1
17	GND	18	DIR
19	GND	20	STEP
21	GND	22	WDATA
23	GND	24	WGATE
25	GND	26	TRK0
27	GND	28	WRPRT
29	GND	30	RDATA
31	GND	32	HDSEL
33	GND	34	DSKCHG

Parallel port

The female DB-25 LPT1 parallel port connector is defined as:

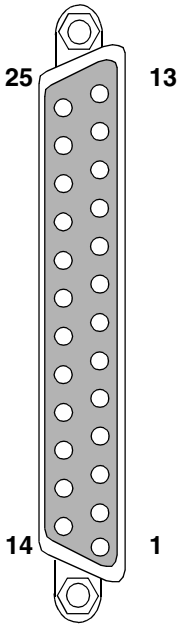


Table F-3. DB-25 pin-out

Pin	Signal	Pin	Signal
1	Strobe	14	Auto line feed
2	DB0	15	Error
3	DB1	16	Initialize printer
4	DB2	17	Select in
5	DB3	18	Signal ground
6	DB4	19	Signal ground
7	DB5	20	Signal ground
8	DB6	21	Signal ground
9	DB7	22	Signal ground
10	Acknowledge	23	Signal ground
11	Busy	24	Signal ground
12	Paper end	25	Signal ground
13	Select		

RS-232/RS-485 port (COM B)

The RS-232/485 serial port is a male DB-9 DTE. For information about how to change jumper settings to configure the EPC-1316 to use the protocol you desire, see *COM B configuration* on page 105.

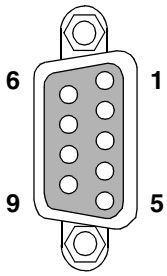


Table F-4. RS-232 pin-out

Pin	Signal	Pin	Signal
1	Carrier detect	6	Data set ready
2	Receive data	7	Request to send
3	Transmit data	8	Clear to send
4	Data terminal ready	9	Ring indicator
5	Signal ground		

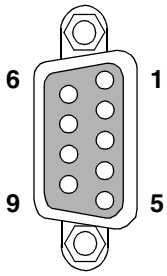


Table F-5. RS-485 pin-out

Pin	Signal	Pin	Signal
1	RXD - ‘ve	6	NC
2	RXD + ‘ve	7	NC
3	TXD + ve	8	NC
4	TXD - ‘ve	9	NC
5	Signal ground		

SCSI-2

The SCSI-2 port is a female 50-conductor .050 center mini-D style connector defined in the following table. To disable the SCSI terminator, see *SCSI termination* on page 105.

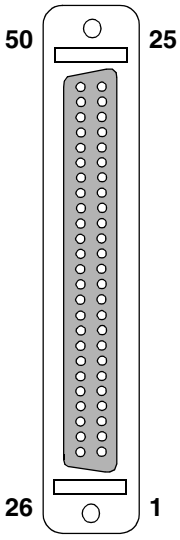


Table F-6. SCSI-2 connector

Pin	Signal	Pin	Signal
1	Signal GND	26	Terminator Power
2	~DB0	27	Signal GND
3	Signal GND	28	Signal GND
4	~DB1	29	Signal GND
5	Signal GND	30	Signal GND
6	~DB2	31	Signal GND
7	Signal GND	32	~ATN
8	~DB3	33	Signal GND
9	Signal GND	34	Signal GND
10	~DB4	35	Signal GND
11	Signal GND	36	~BSY
12	~DB5	37	Signal GND
13	Signal GND	38	~ACK
14	~DB6	39	Signal GND
15	Signal GND	40	~RST
16	~DB7	41	Signal GND
17	Signal GND	42	~MSG
18	~DB8	43	Signal GND
19	Signal GND	44	~SEL
20	Signal GND	45	Signal GND
21	Signal GND	46	~C/D
22	Signal GND	47	Signal GND
23	Signal GND	48	~REQ
24	Signal GND	49	Signal GND
25	Signal GND	50	~I/O

G MSF option board

This appendix describes how to configure and use the optional MSF (Multi-Serial Feature) option board. When reading this file online, you can immediately view information about any installation topic by placing the mouse cursor over a connector name and clicking.

Task	Page
Overview	115
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Overview

The MSF option board is an MSIO (mass storage and I/O expansion) card that provides secondary storage and multiple I/O functions. The MSF option board connects to the Main board via PCI and peripheral buses, and includes these I/O functions:

- Five Serial Ports via front panel DB9 connectors:
  - COM2 routed from the EPC-1316 (RS-232 or RS-485 selectable).
  - COM3 through COM6 provided by on-board UARTs (RS-232).
- PC Compatible Parallel Port routed from EPC-16 (available via on-board header).
- Floppy Disk Drive Interface routed from EPC-16 (available via on-board header).
- Support for EIDE 2.5 inch Hard Disk Drive
- Support for Compact Flash (CF card not included).
- 10/100 Ethernet with RJ45 connector.

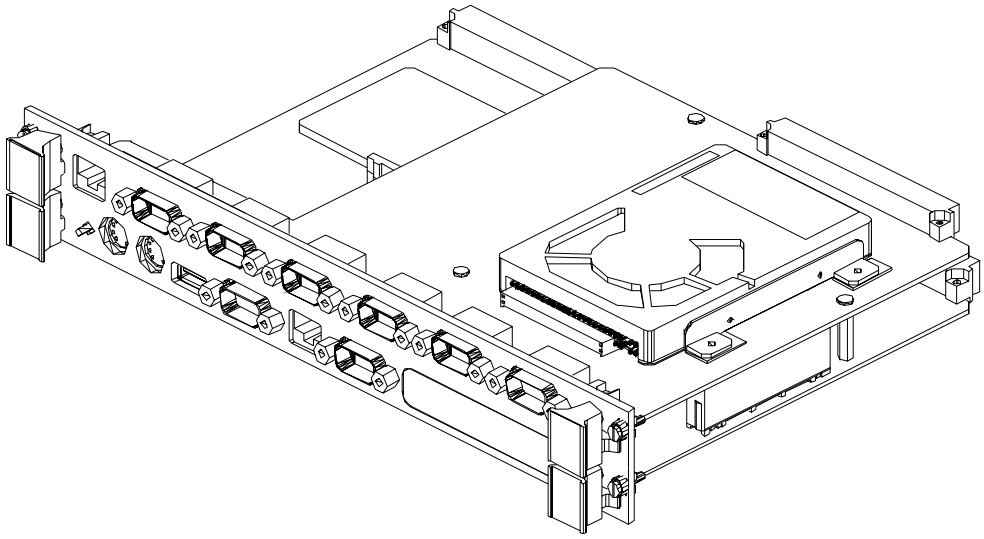


Figure G-1. EPC-1316 with MSF option board

Specifications

Environmental specifications

Table 5-1. EPC-1316 environmental specifications

Characteristic	State	Value
Temperature	Operating	0 to 60°C at point of entry of forced air derated 2°C per 1000 ft. (300 m) over 6600 ft. (2000 m)
	Storage	–40°C +85°C
Humidity	Operating	5% to 95% noncondensing
	Storage	5% to 95% noncondensing
Vibration (excluding hard drive)	Operating	0.15" PP 2.5g (maximum) acceleration over 5–300 Hz sine wave, 1 oct/min sine sweep
	Storage	0.30" PP 5g (maximum) acceleration over 5–300 Hz sine wave, 1 oct/min sine sweep
Shock (excluding hard drive)	Operating	30 g, 11 ms duration
	Storage	50 g, 11 ms duration

Table 5-1. EPC-1316 environmental specifications

Characteristic	State	Value
Safety	RadiSys embedded computers are designed with good EMC practices as intended in “The Council of The European Communities EMC Compatibility Directive” (89/336/EEC). RadiSys currently follows these standards:	
	EN55022	Limits and Methods, ITE
	EN50081-1	Part 1, Emissions
	EN50081-2	Part 2, Emissions
	EN50082-1	Part 1, Immunity (1997)
	EN50082-2	Part 2, Immunity
	EN55024	Immunity, ITE (where applicable)
	EN6100-4-2	Part 4, Section 2, Electrostatic Discharge, ESD
	EN6100-4-3	Part 4, Section 3, Radiated Immunity
	EN6100-4-4	Part 4, Section 4, Electrical Fast Transients (EFT) / Burst - Immunity
	EN6100-4-5	Part 4, Section 5, Surge Immunity
	EN6100-4-6	Part 4, Section 6, Conducted Immunity
	EN6100-4-8	Part 4, Section 11, Voltage Drips and Interruptions
	73/23/EEC	Low Voltage Directive, Including Safety
	FCC Class A certification	

Configuration

To configure the MSF option board, you must complete the steps shown below.

Task	Page
Setting Jumpers on the MSF option board	118
Disconnecting the MSF option board	119
Re-assembling the MSF option board and the Main board	120

Avoid causing ESD damage:

- Remove modules from their antistatic bags only in a static-free environment.
- Perform the installation process (described later in this chapter) only in a static-free environment.
- During the installation process, ensure that power to your system is off. The EPC-1316 is not designed to be inserted or removed while the chassis is powered up.
- During external cable installation, ensure that the cables are not active. The EPC-1316 is not designed for hot insertion of any interface.

The EPC-1316 modules, like most other electronic devices, are susceptible to electrostatic discharge (ESD) damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

⚠ DANGER

If you plan to connect a floppy drive, you must use a RadiSys EXP-FDM (Floppy Disk Module).

Connecting a standard floppy drive can create a fire hazard and may damage or destroy the EPC-1316 baseboard, MSF option board, EXP-FDM, or cable.

Setting Jumpers on the MSF option board

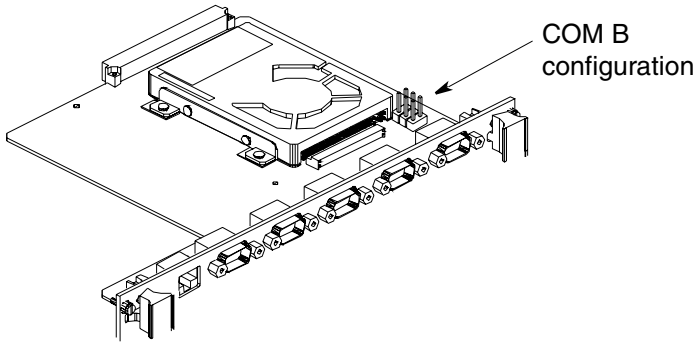


Figure G-2. MSF option board assembly: jumper locations

Jumper pins are labeled from the point of view of looking at the front of the connector.

COM B configuration

Place the COM B jumpers, located next to the RS-232/RS-485 port (COM B) connector on the MSF option board, to set COM B to function as the connector type you desire:

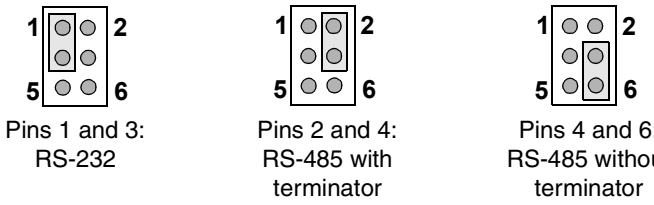


Figure G-3. COM B jumper settings

When in RS-485 mode, you can configure the interface with or without a 100Ohm terminator across the receive channel data pair by connecting pins 2 and 4 together. Noe connecting pins 1 and 3 selects RS485 mode.

Disconnecting the MSF option board

If your EPC-1316 includes the optional MSF option board, you must disassemble the board before performing maintenance (such as replacing the battery) or upgrades (such as adding options) on the EPC-1316.

To separate the MSF option board and the Main board:

1. Remove the EPC-1316 from the VME chassis as described in *Extracting the EPC-1316* on page 13.
2. Remove the screws that attach the MSF option board to the Main board (see Figure G-1 on the next page).
3. Disconnect the boards by pulling apart while keeping them parallel. Continue applying force until the connectors and grips completely disengage.

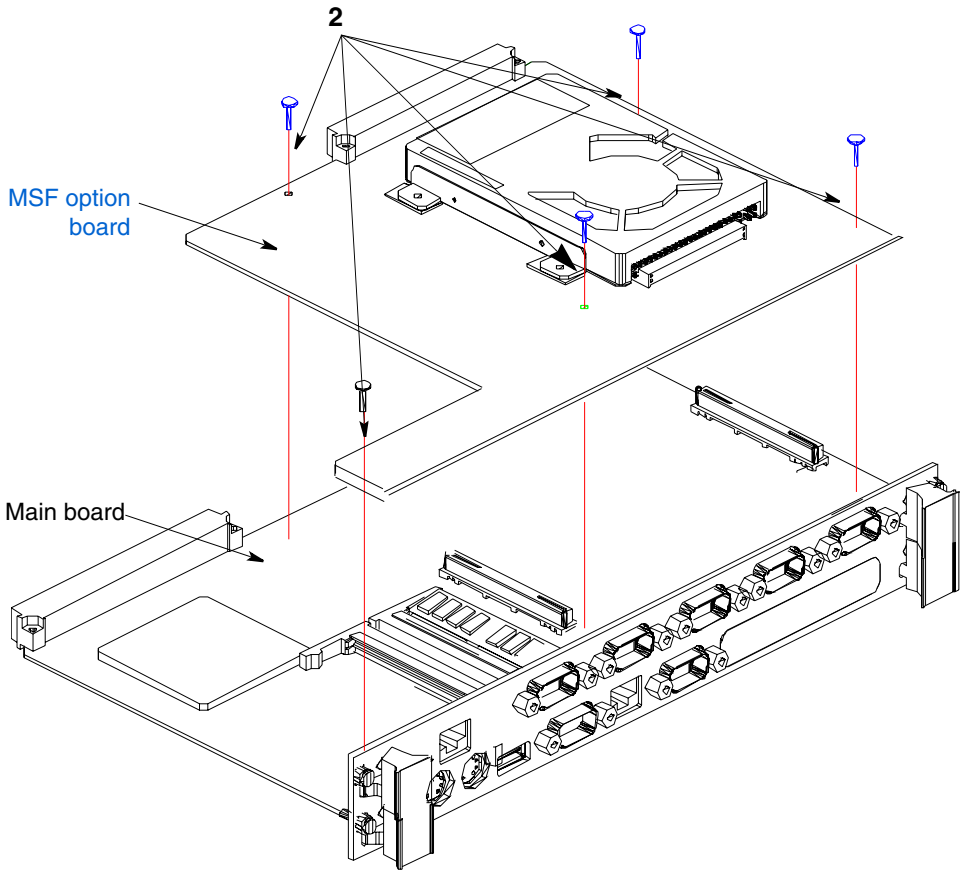


Figure G-4. Disconnecting the MSF option board

Re-assembling the MSF option board and the Main board

1. Remove the EPC-1316 from the VME chassis as described in *Extracting the EPC-1316* on page 12.
2. Connect the main and MSF option boards by pushing while keeping them parallel. Continue applying force until the connectors and grips completely engage.
3. Insert the screws that attach the MSF option board to the main board (see Figure G-5).

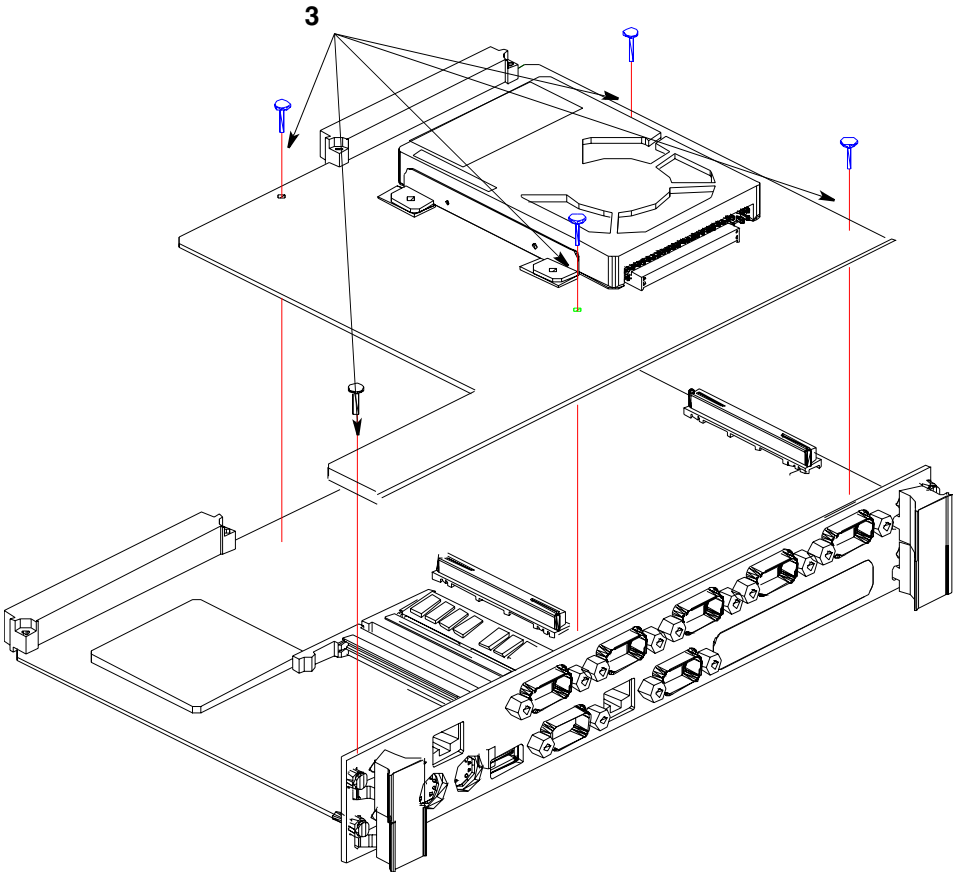


Figure G-5. Attaching the MSF option board to the Main board

BIOS configuration

If you plan to connect a floppy drive to the EXP-FDM floppy connector, be sure to:

- Identify the type of floppy disk drive in the appropriate Legacy Diskette field on the Main menu (see page 18).
- Make floppy disk controller is available for use by enabling the Floppy Disk Controller on the *I/O Device Configuration sub-menu* on page 37.

The MSF option board has the primary IDE interface. If your EPC-1316 includes the MSF option board option, primary IDE is available. To configure the detailed characteristics of the installed IDE drive, select and configure the appropriate Primary/Secondary Master/Slave sub-menus (see page 20).

To identify which port the MSF option board uses, select and configure the appropriate Serial Port field on the *I/O Device Configuration sub-menu* on page 37.

For detailed information about configuring the BIOS, see *Chapter 3, BIOS configuration*.

Organization

Block diagram

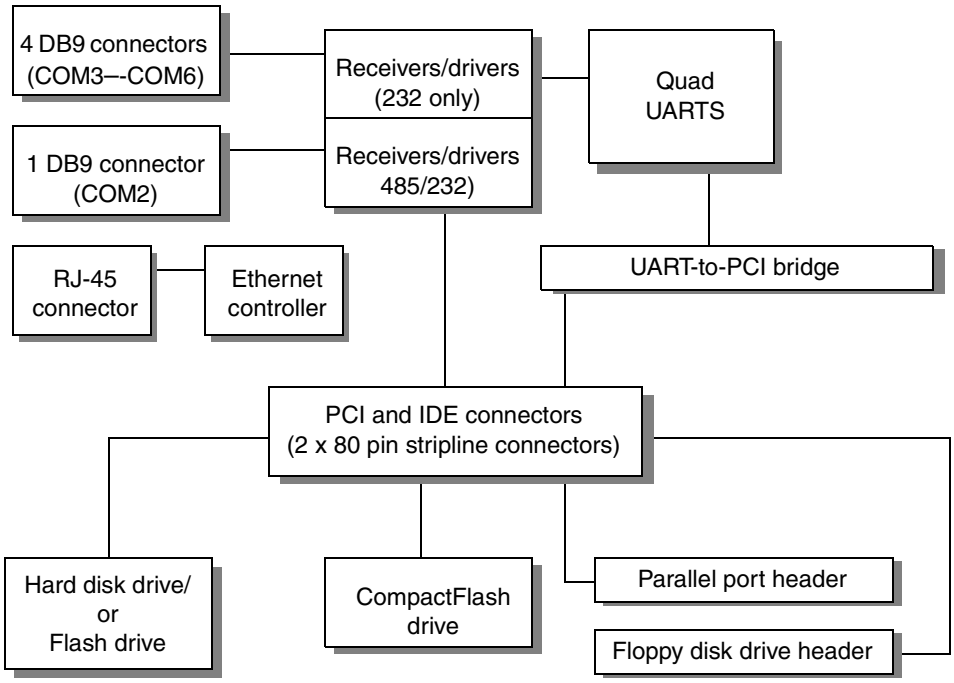


Figure G-6. Block diagram: MSF option board

Feature set

COM B ports

The COM B serial port is driven by the Super I/O on the EPC-1316 through the PCI connector. The signals from the PCI connector are routed to an RS232/RS485 line transceiver. You can configure the interface to be either RS232 or RS485 via a single user-installable jumper. The RS485 terminating resistors are provided via an active termination device, and may be enabled/disabled via a single jumper. “Parking positions” are provided for the jumpers when not in use. For more information about configuring COM B, see *COM B configuration* on page 118

Parallel port

The printer port is a bi-directional IEEE1284-C PC parallel port. The parallel port supports bi-directional communication compatible with the PS/2 definition. It is configured as LPT1, mapped to I/O address 378h–37Fh, and uses interrupt IRQ7. If not needed, LPT1 can be disabled in the BIOS Setup Integrated Peripherals Sub-Menu to free

up the I/O address and interrupt for usage by other expansion products. The parallel port is accessible via the front panel or the P2 connector; these are mutually exclusive.

Serial port interface (COM3 through COM6)

COM3 through COM6 serial ports use SN75185 Texas Instrument receiver/drivers. The signals from the transceivers are routed to the 16C554 Texas Instrument QUAD UART. Refer to section 4.3 for the UART to PCI bus interface. The serial ports use DB9 connectors. The pin assignments are shown in Table 5-6.

PC-compatible parallel interface

The parallel port is accessed by the EPC16 Super I/O through the IDE connector on the MSF card. The port can be configured to run in standard mode, enhanced mode (EPP), or Microsoft high speed mode (ECP). MSDOS and Windows recognize this port as LPT1. The parallel port uses a DB25 pin connector.

Hard drive, Compact Flash drive, and floppy drive

The hard disk drive, the compact flash drive, and the floppy drive communicate to the EPC-1316 through the IDE connector on the MSF option board. The signals from the IDE connector are routed to the hard drive header, compact flash header and the floppy header.

The fast data and edge rates of Enhanced IDE require special attention to signal integrity as the signals travel across the circuit board through multiple connectors and ribbon cable. To help control edge rates and ringing, series resistors are used on all IDE signals.

Hard drive interface

The hard drive follows the EIDE standard.

Compact Flash drive interface

The compact flash follows the EIDE standard.

Floppy disk Interface

The EPC-1316 accesses the floppy drive through the IDE connector on the MSF option board. The floppy disk connector supports 3.5", 1.44MByte, 2.88MByte, or 720KByte floppy disk, depending on the floppy disk drive.

UART-to-PCI bridge

The UART to PCI Bridge interface is a PCI target that conforms to PCI Specification 2.1.

Ethernet controller

An Intel 82559ER Fast Ethernet controller (µBGA packaging) incorporates internal MAC (media access controller) and PHY (Physical Interface) interfaces that provide support for 10BASE-T or 100BASE-TX connections. The Ethernet controller uses PCI interrupt C, ~REQ/~GNT arbitration pair 3, and has a standard PCI 2.1 compliant configuration space, allowing system identification and configuration.

The PHY enables direct connection to the network media using a 25 MHz, 25 ppm crystal to derive its internal transmit digital clocks. A compatible, integrated magnetics inside the

RJ45 connector interfaces the 82559ER with the RJ45 connector, located on the top right edge of the board. In 100BASE-TX mode, the analog subsection of the PHY performs two functions:

- Converts received analog data from the RD pair into a digital 125 Mbps stream, recovering both clock and data.
- Converts a digital 125 Mbps stream into the proper format and drive it through the TD pair into the physical medium.

The 82559ER provides Link and Activity LED indicators capable of sinking 10 mA. The 82559ER drives the LINK and ACTIVITY LEDs integral to the RJ45 connector directly. The Ethernet controller uses a RJ45 located on the front panel. For more information about the Ethernet connector and the LEDs, see *Ethernet* on page 126.

Connectors

The MSF option board product includes these connectors and jumpers:

Connector	Page
Connector locations	123
Compact Flash header	124
EIDE (primary)	125
Ethernet	126
EXP-FDM floppy	127
Parallel port	128
RS-232/RS-485 port (COM B)	128

Connector locations

Figure G-7 shows the locations of the connectors on the EPC-1316 MSF option boardMSF option board.

For information about installing peripherals and jumper settings, see *Configuration*.

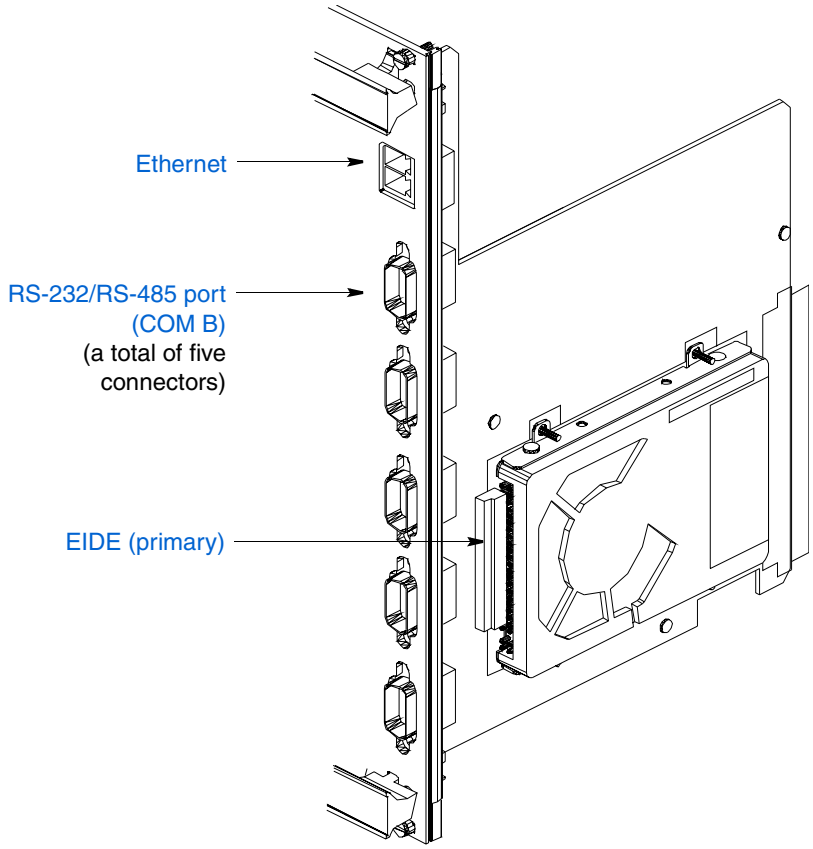


Figure G-7. MSF option board: connectors

Compact Flash header

Table E-1. Compact Flash header

Pin	Signal	Pin	Signal
1	~RST	2	Signal GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	Sgnal GND	20	NC
21	DRQ	22	Signal GND
23	~IOW	24	Signal GND
25	~IOR	26	Signal GND
27	ORDY	28	CSEL

Table E-1. Compact Flash header

Pin	Signal	Pin	Signal
29	~DAK	30	Signal GND
31	IRQ	32	NC
33	A1	34	Signal GND
35	A0	36	A2
37	~CS0	38	~CS1
39	ACT	40	Signal GND
41	+5 Volts	42	+5 Volts
43	Signal GND	44	Signal GND

EIDE (primary)

The Primary EIDE Connector is a male 44-pin right-angle header located on the MSF option board. The pins and signals are defined as:

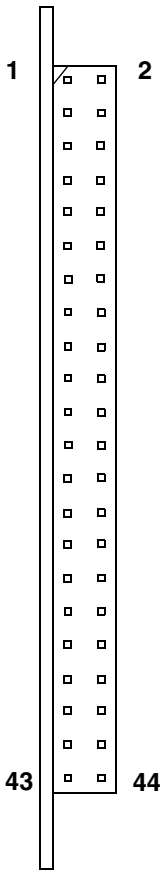


Table G-1. Primary EIDE connector

Pin	Signal	Pin	Signal
1	~RST	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	N.C.
21	DRQ	22	GND
23	~IOW	24	GND
25	~IOR	26	GND
27	IORDY	28	PPU
29	~DAK	30	GND
31	IRQ	32	N.C.
33	A1	34	N.C.
35	A0	36	A2
37	~CS0	38	~CS1
39	ACT	40	GND
41	+5 Volts	42	+5 Volts
43	GND	44	GND

Ethernet

The DTE RJ-45 phone jack supplies the 100/10BASE-T interface to the Ethernet controller.

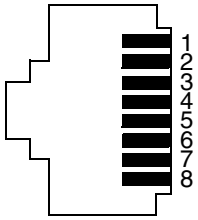


Table G-2. RJ45 phone jack pin-out

Pin	Signal	Pin	Signal
1	Transmit+	5	Center tap TX
2	Transmit–	6	Receive–
3	Receive+	7	Center tap RX
4	Center tap TX	8	Center tap RX

The Ethernet connector also includes these LEDs:

LED	Color	Description
LINK	Green	Indicates the Ethernet link status. When on, the adapter has a valid link on its network connection and is ready for normal operation (10BASE–T link or 100BASE–TX link). When off, the adapter did not find a valid 10/100BASE-TX link on its network connection; transmit and receive are not possible.
ACT	Green	Indicates Ethernet activity. The LED indicates the transmit or receive activity for the 10BASE–T or 100BASE–TX network connections. When on, a packet is being transmitted or received. When off, no transmission activity occurs.

EXP-FDM floppy

The floppy disk drive connector is a male 34-pin header located on the front panel of the MSF option board. The pins and signals are defined as:

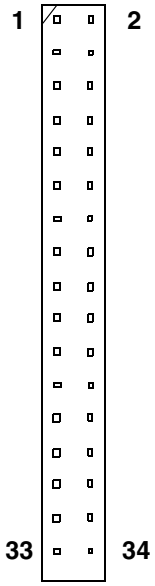


Table G-3. EXP-FDM floppy connector

Pin	Signal	Pin	Signal
1	GND	2	DENSEL
3	N.C.	4	N.C.
5	N.C.	6	RATE0
7	5 Volts	8	~INDEX
9	5 Volts	10	N.C.
11	5 Volts	12	~DS0
13	GND	14	N.C.
15	GND	16	~ME0
17	GND	18	~DIR
19	GND	20	~STEP
21	GND	22	~WRDATA
23	GND	24	~WE
25	GND	26	~TRK0
27	GND	28	~WP
29	GND	30	:~RDATA
31	GND	32	~HDSEL
33	GND	34	~DSKCHG

Parallel port

The female DB-25 LPT1 parallel port connector is defined as:

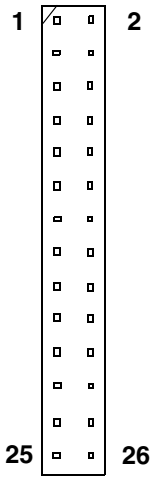


Table G-4. DB-25 pin-out

Pin	Signal	Pin	Signal
1	~STB (strobe)	14	~AF (auto line feed)
2	DB0	15	~ERR (error)
3	DB1	16	~INIT (initialize printer)
4	DB2	17	~SELIN (select in)
5	DB3	18	GND (signal ground)
6	DB4	19	GND (signal ground)
7	DB5	20	GND (signal ground)
8	DB6	21	GND (signal ground)
9	DB7	22	GND (signal ground)
10	~ACK (acknowledge)	23	GND (signal ground)
11	BUSY	24	GND (signal ground)
12	PE (paper end)	25	GND (signal ground)
13	ALCT (select)	26	GND (signal ground)

RS-232/RS-485 port (COM B)

The five RS-232/485 serial ports are male DB-9 DTEs. For information about how to change jumper settings to configure the EPC-1316 to use the protocol you desire, see *COM B configuration* on page 118.

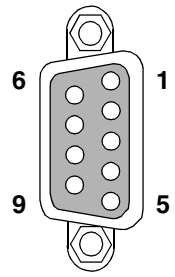


Table G-5. RS-232 pin-out

Pin	Signal	Name	Pin	Signal	Name
1	DCD	Carrier detect	6	DSR	Data set ready
2	RXD	Receive data	7	RTS	Request to send
3	TXD	Transmit data	8	CTS	Clear to send
4	DTR	Data terminal ready	9	RI	Ring indicator
5	GND	Signal ground			

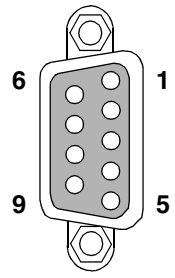


Table G-6. RS-485 pin-out

Pin	Signal	Pin	Signal
1	RXD - 've	6	NC
2	RXD + 've	7	NC
3	TXD + ve	8	NC
4	TXD - ve	9	NC
5	Signal ground		

H Flash disk module

This appendix describes how to install the optional Flash module. When reading this file online, you can immediately view information about any installation topic by placing the mouse cursor over a topic and clicking.

Task	Page
Installing the Flash module	129
Disconnecting the Flash module	131
Organization	132
Connectors	134

Installing the Flash module

Installing the CompactFlash card on the Flash module

Before you can install the Flash module on the EPC-1316, you must insert a CompactFlash card:

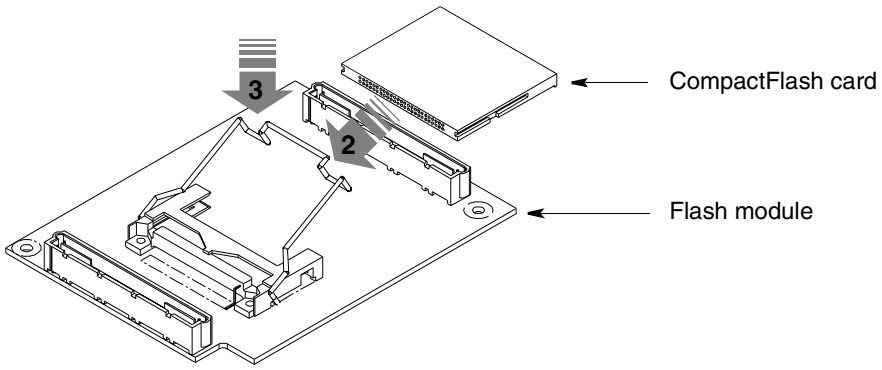


Figure H-1. Installing the CompactFlash card on the Flash module

1. Lift up the metal clip that secures the CompactFlash card.
2. Slide the CompactFlash card into the slot.
3. Push down the metal clip to secure the CompactFlash card.

Installing the Flash module on the Main board

You install the Flash module on the EPC-1316's Main board as shown below.

You cannot have a PMC module and a Flash module on the EPC-1316 at the same time.

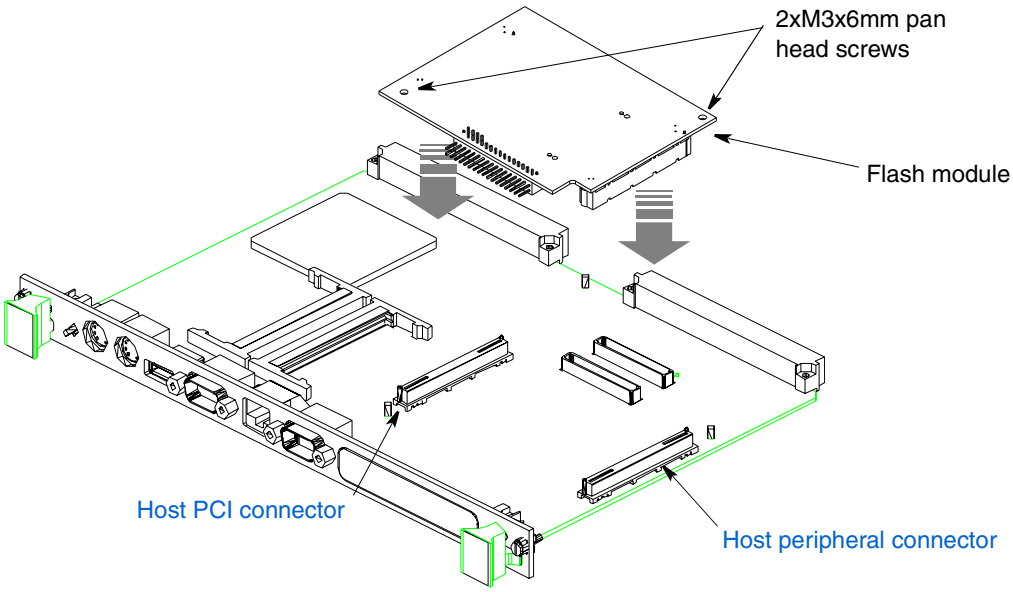


Figure H-2. Installing the optional Flash module on the EPC-1316

To install a Flash module:

Avoid causing ESD damage:

- Remove modules from their antistatic bags only in a static-free environment.
- Perform the installation process (described later in this chapter) only in a static-free environment.
- During the installation process, ensure that power to your system is off. The EPC-1316 is not designed to be inserted or removed while the chassis is powered up.
- During external cable installation, ensure that the cables are not active. The EPC-1316 is not designed for hot insertion of any interface.

The EPC-1316 modules, like most other electronic devices, are susceptible to electrostatic discharge (ESD) damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

1. Remove the EPC-1316 from the VME chassis as described in *Extracting the EPC-1316* on page 13.
2. If your EPC-1316 includes the optional Carrier board, disengage the Main and Carrier boards as described in *Disconnecting the MSIO Carrier Board* on page 106.

   If you install a Flash module on the EPC-1316, you cannot re-attach the Carrier board. The Flash module is available only for EPC-1316s not fitted with the MSIO Carrier Board or PMC module options.

3. Attach to the EPC-1316 2xM3 standoffs as provided in the accessory kit.
4. Align the Host PCI and Peripheral Connectors on the Flash module and Main board, then push the boards together while keeping them parallel. Continue applying force until the connectors completely engage.

5. Insert and tighten the screws on the Flash module.
6. Replace the EPC-1316 in the VME chassis as described in *Inserting the EPC-1316* on page 11.
7. Re-configure the EPC-1316 to include the Flash module, as described in *Chapter 3, BIOS configuration*.

Disconnecting the Flash module

If your EPC-1316 includes the optional Flash module, you must disassemble the board before performing maintenance (such as replacing the battery) or upgrades (such as adding options) on the EPC-1316.

To separate the Flash module and the Main board:

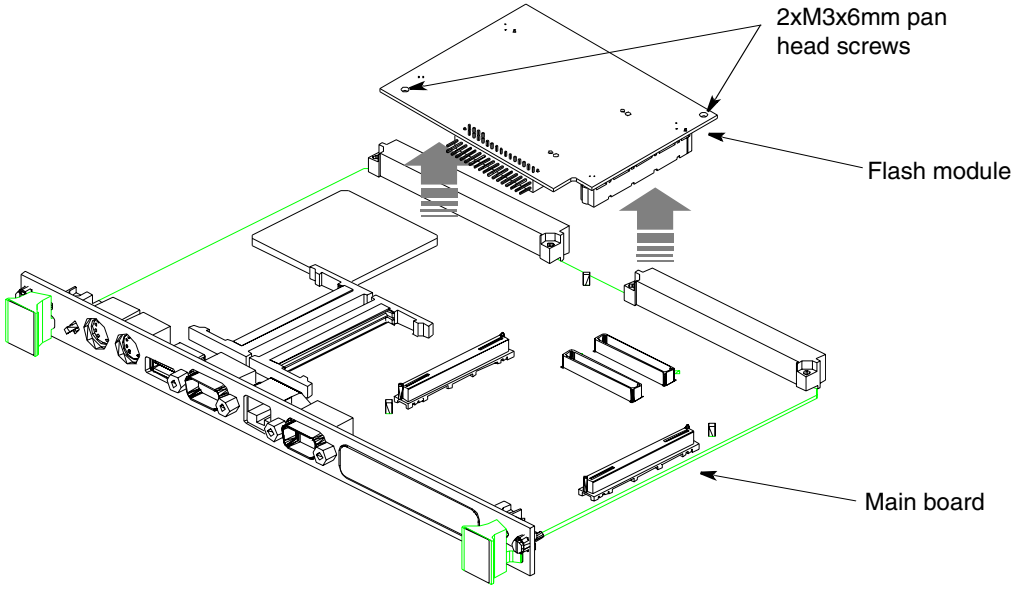


Figure H-3. Disconnecting the optional Flash module

1. Remove the EPC-1316 from the VME chassis as described in *Extracting the EPC-1316* on page 13.
2. Remove the screws on the Flash module.
3. Pull the boards apart while keeping them parallel. Continue applying force until the connectors completely disengage.

Organization

Block diagram

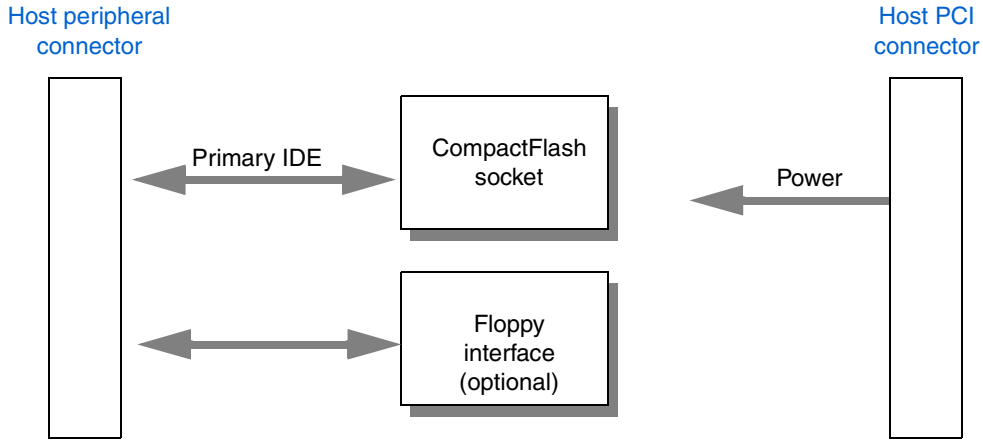


Figure H-4. Block diagram: Flash module

Feature set

The Compact Flash module is an optional add-on card for the EPC-1316 board. This board provides, as the standard feature, an IDE interface to the SanDisk Compact Flash memory module (via board mounting position) and, optionally, a Floppy Disk Drive Interface (no power provided to cable) for debug or future expansion.

The Compact Flash board connects with the host EPC board via two 80 way stripline stacking connectors and is secured by screws, so that the two boards form a single assembly. The module includes a retaining clip to provide mechanical stability in the event of vibration or handling.

Specifications

Table H-1. Flash module environmental specifications

Characteristic	State	Value
Temperature	Operating	0–55°C at point of entry of forced air derated 2°C per 1000 ft. (300 m) over 12,000 ft. (3600 m)
	Storage	–40°C –85°C
Humidity	Operating	5%–95% noncondensing
	Storage	5%–95% noncondensing
Vibration	Operating	2.5 g acceleration over 5–2000 Hz sine wave (P-P), 1 oct/min sine sweep
	Storage	5 g acceleration over 5–2 kHz sine wave (P-P), 1 oct/min sine sweep
Shock	Operating	30 g, 11 ms duration, half-sine shock pulse
	Storage	50 g, 11 ms duration, half-sine shock pulse

Table H-2. Flash module power supply specifications

Characteristic	Value
Current	+5V @ 150mA (IDE Compact Flash drive interface only)

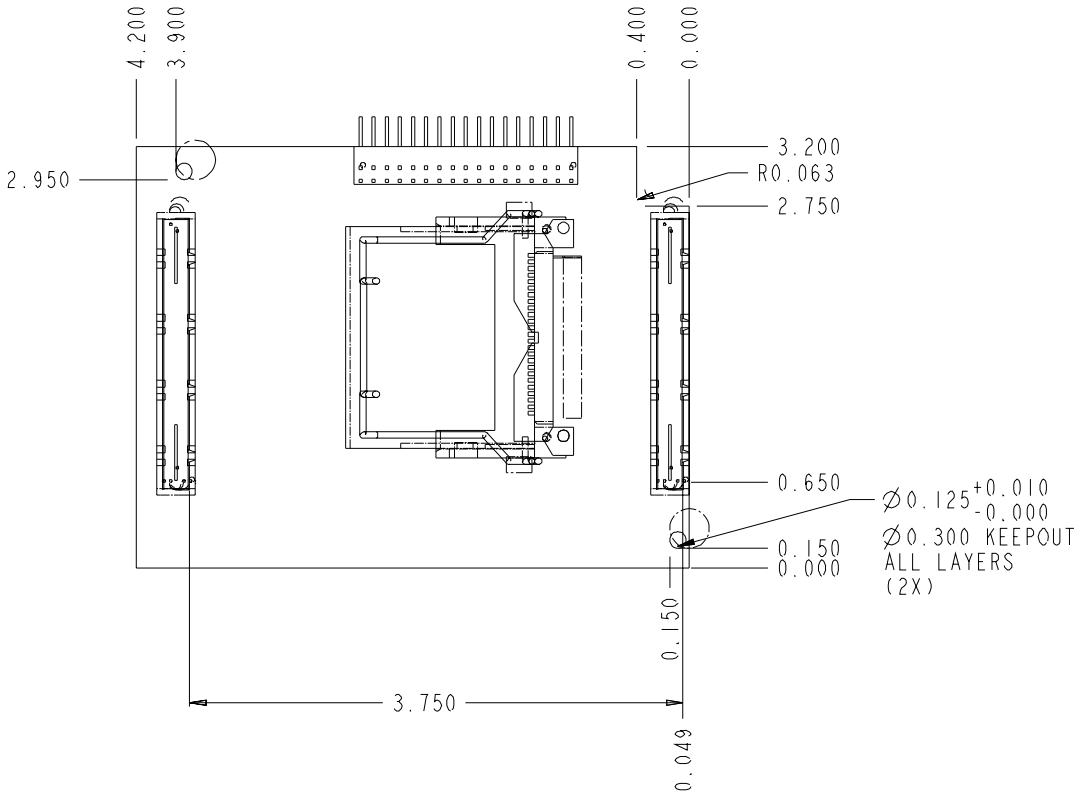


Figure H-5. Flash module dimensions

Connectors

The Flash module includes these connectors:

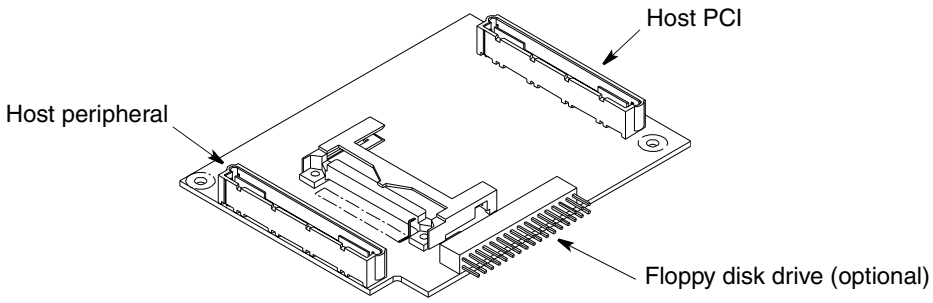


Figure H-6. Flash module connectors

Floppy disk drive (optional)

The floppy disk drive connector is male 34-pin connector defined as:

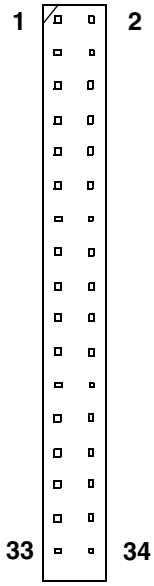


Table H-3. Standard floppy pin-out

Pin	Signal	Pin	Signal
1	GND	2	DENSEL
3	GND	4	N.C.
5	GND	6	DRATE0
7	GND	8	~INDEX
9	GND	10	~MTR1
11	GND	12	~DS0
13	GND	14	~DS1
15	GND	16	~MTR0
17	GND	18	~DIR
19	GND	20	~STEP
21	GND	22	~WDATA
23	GND	24	~WGATE
25	GND	26	~TRK0
27	GND	28	~WRPRT
29	GND	30	~RDATA
31	GND	32	~HDSEL
33	GND	34	~DSKCHG

Host peripheral

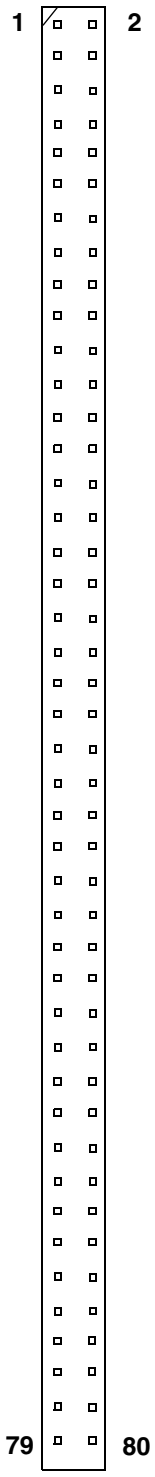


Table H-4. Host peripheral connector

Pin	Signal	Pin	Signal	Function
1	FD:DENSEL	2	FD:~WDATA	Floppy disk interface
3	FD:~INDEX	4	FD:~WGATE	
5	+12V	6	–12V	
7	FD:~DS1	8	FD:~TRK0	
9	FD:~MTR	10	FD:~WRPRT	
11	FD:~DIR	12	FD:~RDATA	
13	FD:~STEP	14	FD:~HDSEL	
15	FD:DRATE0	16	FD:~DSKCHG	
17	+5 Volts	18	+5 Volts	
19	+5 Volts	20	+5 Volts	
21	PR:~Strobe	22	NC	Parallel port
23	PR:PD0	24	PR:PD4	
25	PR:PD1	26	PR:PD5	
27	PR:PD2	28	PR:PD6	
29	PR:PD3	30	PR:PD7	
31	PR:~ACK	32	PR:~AF (Auto Feed)	
33	PR:BUSY	34	PR:~ERR	
35	PR:PE (Paper end)	36	PR:~INIT	
37	PR:SLCT	38	PR:~SLIN	
39	+5 Volts	40	+5 Volts	IDE interface
41	+5 Volts	42	+5 Volts	
43	PR:D0	44	PR:PD8	
45	PR:D1	46	PR:PD9	
47	PR:D2	48	PR:PD10	
49	PR:D3	50	PR:PD11	
51	PR:D4	52	PR:PD12	
53	PR:D5	54	PR:PD13	
55	PR:D6	56	PR:PD14	
57	PR:D7	58	PR:PD15	
59	Signal GND	60	+5 Volts	
61	IDE:DRQ	62	+5 Volts	
63	IDE:~IOW	64	AT:~RSTDRV	
65	IDE:~IOR	66	FD:~DS0	
67	IDE:IORDY	68	FD:ME0	
69	IDE:~DAK	70	Signal GND	
71	AT.IRQ14	72	NC	
73	IDE:A1	74	NC	
75	IDE:A0	76	IDE:SA2	
77	IDE:~CS0	78	IDE:~CS1	
79	IDE:~ACT	80	NC	

Table H-5. Host peripheral connector power pins

Pin	Signal	Pin	Signal
81	GND	82	GND
83	GND	84	GND
85	NC	86	GND
87	GND	88	GND
89	GND	90	NC
91	GND	92	GND
93	GND	94	GND
95	NC	96	+5V
97	+5V	98	+5V
99	+5V		

Host PCI

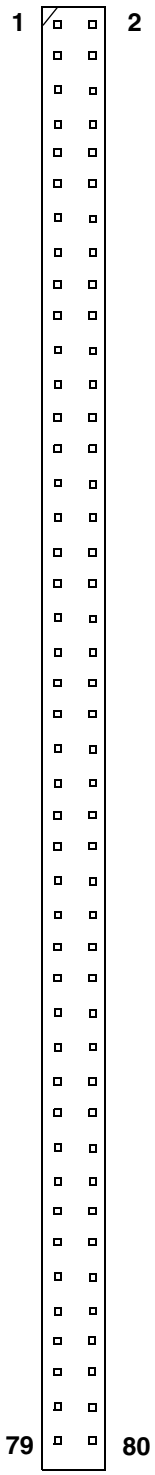


Table H-6. Host PCI connector

Pin	Signal	Pin	Signal	Function
1	PCI:~IRQC	2	PCI:~IRQB	Floppy disk interface
3	PCI:~IRQA	4	PCI:~IRQD	
5	+12V	6	–12V	
7	$PCI:CLK0	8	$PCI:CLK3	
9	NC	10	NC	
11	PCI:~GNT3	12	PCI:~REQ3	
13	PCI:AD0	14	PCI:AD1	
15	PCI:AD2	16	PCI:AD3	
17	PCI:AD4	18	PCI:AD5	
19	PCI:AD6	20	PCI:AD7	
21	PCI:AD8	22	PCI:AD9	Parallel port
23	PCI:AD10	24	PCI:AD11	
25	PCI:AD12	26	PCI:AD13	
27	PCI:AD14	28	PCI:AD15	
29	PCI:AD16	30	PCI:AD17	
31	PCI:AD18	32	PCI:AD19	
33	PCI:AD20	34	PCI:AD21	
35	PCI:AD22	36	PCI:AD23	
37	PCI:AD24	38	PCI:AD25	
39	PCI:AD26	40	PCI:AD27	IDE interface
41	PCI:AD28	42	PCI:AD29	
43	PCI:AD30	44	PCI:AD31	
45	NC	46	NC	
47	PCI:~FRAME	48	PCI:~STOP	
49	PCI:~IRDY	50	PCI:~DEVSEL	
51	PCI:~LOCK	52	PCI:~SERR	
53	PCI:~TRDY	54	PCI:~PERR	
55	PCI:C/~BE0	56	PCI:C/~BE1	
57	PCI:C/~BE2	58	PCI:C/~BE3	
59	PCI:PAR	60	PCI:~RST	
61	NC	62	NC	
63	Reserved	64	Reserved	
65	Reserved	66	Reserved	
67	Reserved	68	Reserved	
69	Reserved	70	Reserved	
71	Reserved	72	Reserved	
73	~RXD2	74	~R12	
75	~DCD2	76	~DSR2	
77	~RTS2	78	~TXD2	
79	~DTR2	80	~CTS2	

Table H-7. Host PCI connector power pins

Pin	Signal	Pin	Signal
81	GND	82	GND
83	GND	84	GND
85	NC	86	GND
87	GND	88	GND
89	GND	90	NC
91	GND	92	GND
93	GND	94	GND
95	NC	96	+5V
97	+5V	98	+5V
99	+5V		

I PMC modules

The EPC-1316 can accept most PMC types excluding those that either require a disk BIOS in the EPC or do not fit by form factor. The EPC-1316 accepts only 5V PCI signaling environment. PMC modules which do not have the 5V PCI signaling are mechanically prevented from being inserted.

You cannot have a PMC module and a Flash disk module on the EPC-1316 at the same time.

Installing a PMC module on the Main board

You can install a PMC module to the EPC-1316's Main board as shown below.

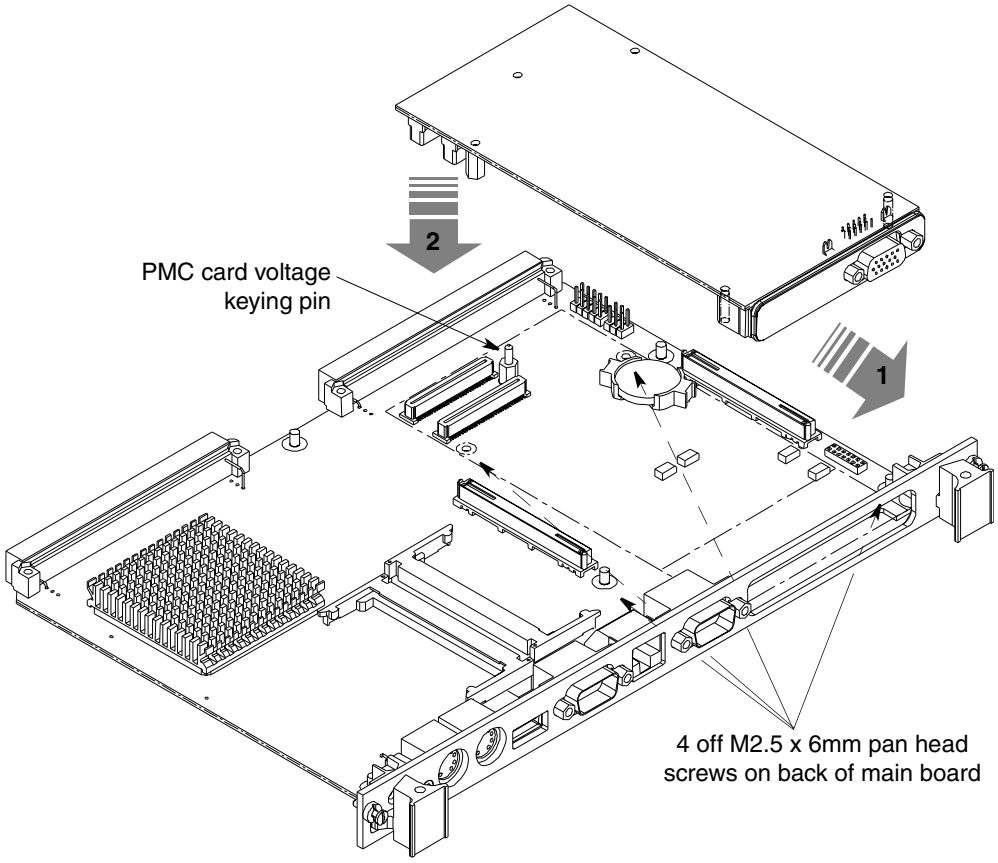


Figure I-1. Inserting a PMC module

To install a PMC module:

Avoid causing ESD damage:

- Remove modules from their antistatic bags only in a static-free environment.
- Perform the installation process (described later in this chapter) only in a static-free environment.
- During the installation process, ensure that power to your system is off. The EPC-1316 is not designed to be inserted or removed while the chassis is powered up.
- During external cable installation, ensure that the cables are not active. The EPC-1316 is not designed for hot insertion of any interface.

The EPC-1316 modules, like most other electronic devices, are susceptible to electrostatic discharge (ESD) damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

1. Turn off the power.
2. Remove the EPC-1316 from the VME chassis as described in *Extracting the EPC-1316* on page 13.
3. If your EPC-1316 includes the optional Carrier board, disengage the main and carrier boards as described in *Disconnecting the MSIO Carrier Board* on page 106.
4. Remove and save the blank face plate from the PMC slot in the EPC-1316 face plate.
5. Position the PMC bezel through the PMC slot on the front panel, then push the rear connectors into the main board.
6. Insert and tighten the screws on the back of the Main board.
7. If your EPC-1316 includes the optional Carrier board, re-assemble the EPC-1316 as described in *Re-assembling the MSIO Carrier Board and the Main board* on page 107.
8. Replace the EPC-1316 in the VME chassis as described in *Inserting the EPC-1316* on page 11.

Disconnecting the PMC module

If your EPC-1316 includes an optional PMC module, you must disassemble the board before performing maintenance (such as replacing the battery) or upgrades (such as adding options) on the EPC-1316.

To separate the PMC module and the Main board:

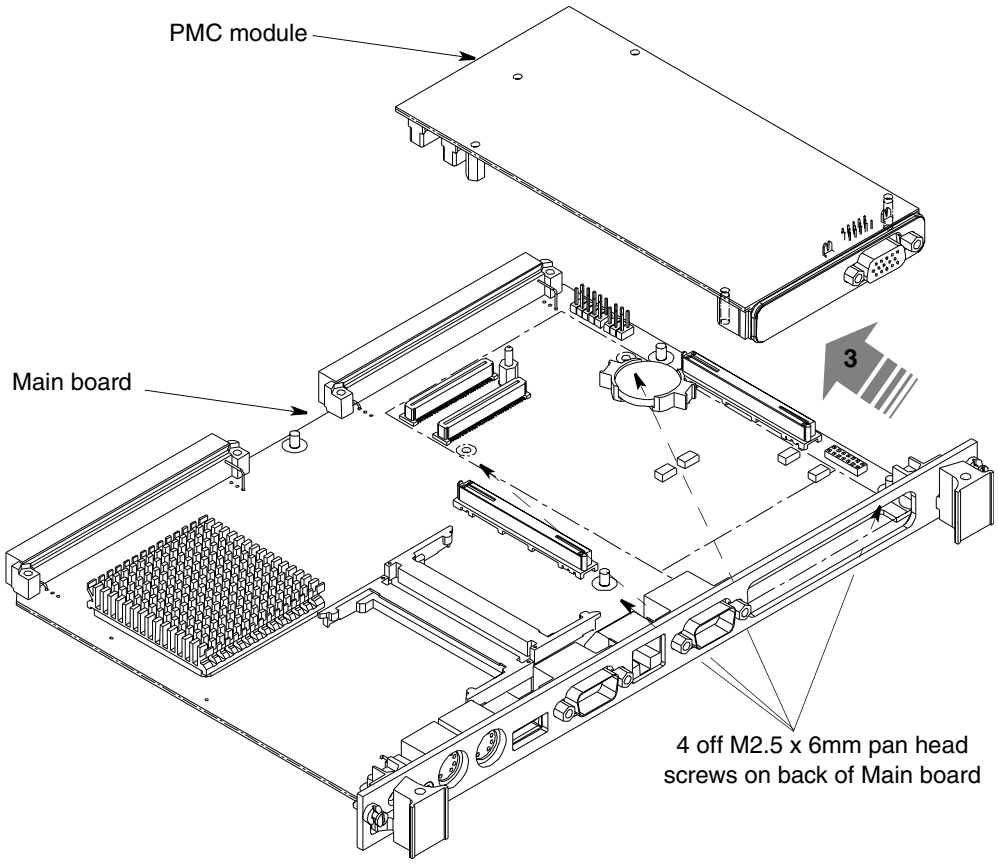


Figure I-2. Disconnecting an optional PMC module

1. Remove the EPC-1316 from the VME chassis as described in *Extracting the EPC-1316* on page 13.
2. Remove screws on the back of the Main board.
3. Pull the boards apart while keeping them parallel. Continue applying force until the connectors completely disengage.

J Installing and configuring RomPilot

This appendix describes how to install, configure, and enable RomPilot software.

RomPilot tools manage an EPC-1316 system from a remote location using network connections to communicate. RomPilot consists of:

- **Management Workstation (MWA) software**: A software application installed on your system (the client) that you use to remotely manage remote systems (servers).
- **RomPilot image**: Code integrated into the BIOS of remote systems. The EPC-1316 already contains the RomPilot image; you need only enable it.

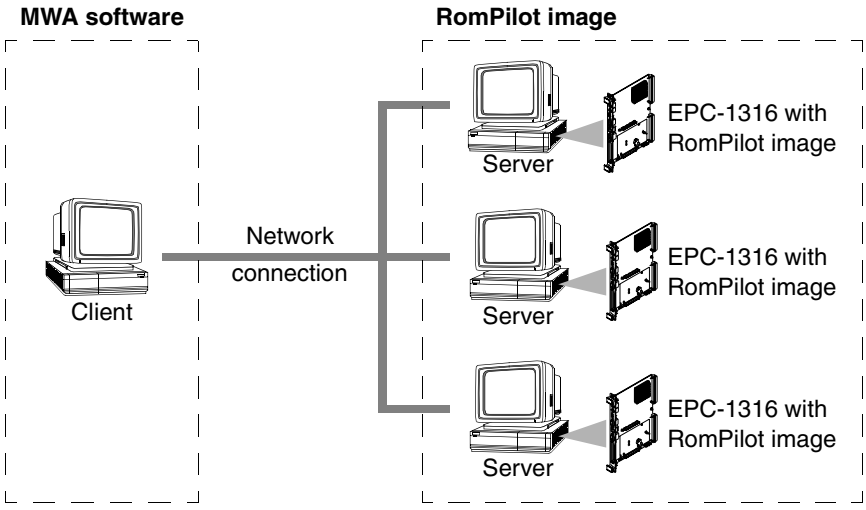


Figure J-1. Where RomPilot components reside

When reading this file online, you can immediately view information about any RomPilot topic by placing the mouse cursor over a topic name and clicking:

Task	Page
Configuring and enabling the RomPilot image	144
Enable RomPilot	148
Configuring the client	149
Link the client with server(s)	150

About RomPilot

RomPilot provides the tools you need to remotely manage an EPC-1316 system, including BIOS, configuration, and startup. RomPilot is compatible with many PCI network adapters. After you link the client and the server(s), you can:

- Store information about all server systems.
- Automatically log and monitor server's boot process.
- Pause and step through the server's POST.
- Access the server's DMI, ESCD, CMOS, PCI, and sector level disk information.
- Reboot the server.
- Upload and execute PLMs (Phoenix Loadable Modules).

Configuring and enabling the RomPilot image

The EPC-1316's BIOS already contains the RomPilot image. Follow the directions in this section to configure and enable RomPilot. You must complete these steps on each server you want to manage remotely..

Until you configure the RomPilot image and the client communicates with a server, the following message displays during the boot process:

```
RomPilot reports error #26
```

Do one of these:

- Press the Esc key to move to the previous window.
- Select Abort to halt the installation.

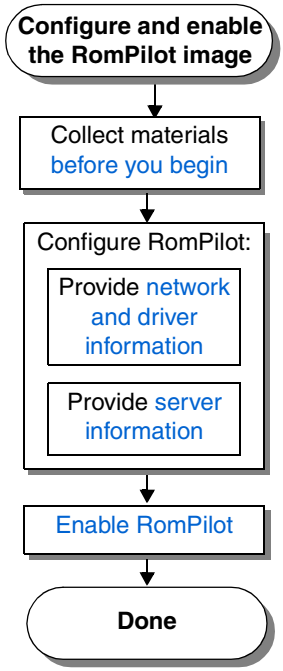


Figure J-2. Configuring and enabling RomPilot

Before you begin

Collect the following prior to starting:

- The RomPilot install disk. To obtain the install disk, see the RadiSys web site.
- (Optional) A DOS floppy to boot your system to a DOS prompt.
- A PCI network adapter.

  RadiSys has validated an Intel 82558-based Ethernet adapter with the EPC-1316.

- An IP and gateway address to assign to the server. You can also attach a Dynamic Host Configuration Protocol (DHCP) server to a DHCP-capable network. This assigns an IP address at the time of connection.
- The client's IP address.
- The correct network driver. The driver must be a Netware driver, posses a "LAN" extension, and be less than 150,000 bytes.

Configure RomPilot

To configure the RomPilot image, you must provide information required to complete a series of configuration windows.

1. Boot the server to MS-DOS.

   Ensure that MS-DOS does not load any memory managers.

2. Insert the RomPilot install disk into the floppy drive and enter this command:

   ```
   install
   ```

   The first time you execute the RomPilot image configuration program, the following message may display:

   ```
   RomPilot install data is corrupt. Using defaults.
   ```

   This is normal; press the Enter key to continue configuration.

   The Main menu displays:

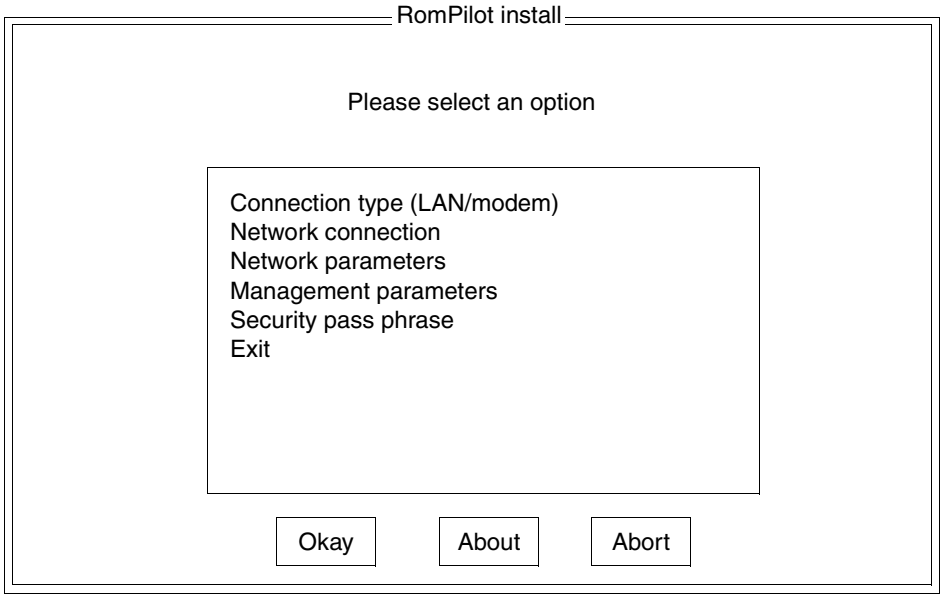


Figure J-3. RomPilot Main menu

From this menu you specify the network, driver, and server information required for RomPilot by completing each option on the screen. The first options specify network and driver information, while the second series specifies server information.

To select an option, use the tab key. To select the Okay button, you can tab to that button, then press the Enter key or, as a shortcut, you can press the enter key twice.

Network and driver information

1. Select Network Adapter (the default) as the type of connection that the server uses to communicate with the client.

   The Network Adapter window displays.

2. Identify the network adapter you want to use with RomPilot.

   The Network Driver Window displays.

3. Specify the driver you want to use with the server's network adapter. You can enter a path into the top field; use Refresh to display potential drivers.

   The Driver Load String Window displays.

4. Enter the load string for the network driver. You can edit the default load string, if needed although, in most cases, you can use the default value.

   The Information/Verification window displays.

5. Confirm your selections for the network adapter and driver.

   You can return to any sub-menu and change values prior to confirming your selections.

   A few moments pass as the network adapter links with the server. When finished, the DHCP window displays.

Server information

1. Select how you want to specify the server's IP address:

   - Select DHCP to use a DHCP server. If you select this option, you will not need a specific IP address for the server.

     The Drivers Parameters window displays.

   - Select an option other than DHCP.

     The Machine Details window displays, where you specify the server's IP address, Subnet mask, and Gateway address.

     The Driver Parameters window displays, where you specify the network adapter's buffer details. The default settings are sufficient for most situations.

     The buffer size must be a minimum of 2100.

   The Machine Name window displays.

2. Assign a unique name to the RomPilot server. The client uses the this name to distinguish between different servers.

   The Management Machines window displays.

3. Complete the IP Address, Application Type, and Timeout fields.

   Use a maximum of three client machines to manage the servers on a network. Only one client can communicate with one specific server at one specific time. Using a Timeout prioritizes the clients.

   The Reset Traps window displays

4. Select the default settings in the Reset Traps, Error Traps, Boot Traps, and 2nd SNMP port windows:

   The Pass Phrase window displays.

5. Enter a pass-phrase.

   The pass-phrase must contain 1 to 64 characters. This is the same pass-phrase that links the the server to the client.

After you confirm the pass-phrase, the configuration program reads the BIOS into a file. It then inserts the driver and the configuration information into the BIOS. The customized BIOS automatically reflashes into the server.

If you execute the install from a floppy disk, this may take a couple of minutes.

During this process, a series of messages displays:

```
Reading BIOS from ROM into a file.
Inserting driver into BIOS file.
Writing BIOS from file to ROM.
```

After BIOS reflash, the final information window displays and the server reboots.

Enable RomPilot

To enable RomPilot:

1. Reboot the server.
2. During the boot process, press F2 to enter BIOS Setup.
3. Navigate to the BIOS main menu setup screen. See *Main menu* on page 18, for specific instructions.
4. Select RomPilot.
5. Change setting to Enabled.
6. Exit BIOS setup and continue the Boot process. The server is now ready to communicate with the client.

Configuring the client

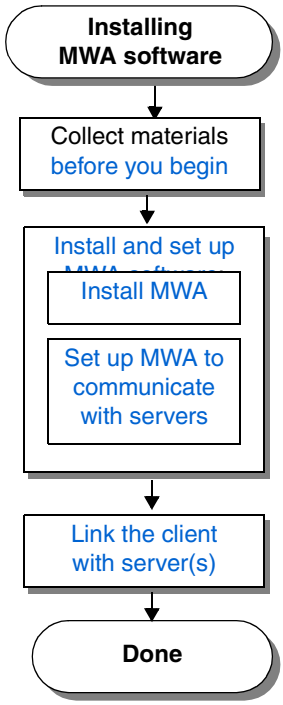


Figure J-4. Installing RomPilot's MWA software

Before you begin

System requirements

The client machine requires:

- Windows 95, Windows 98 or Windows NT.
- A minimum 5 MB of free disk space.

Installation and configuration requirements

Collect the following prior to starting:

- The client's IP address.
- The server's name.
- The server's Pass-Phrase.

The client must be connected to the same network as the server.

Install and set up MWA software

Install MWA

1. Insert the MWA install disk into the client's floppy drive. To obtain the install disk, see the RadiSys web site.
2. Double-click Setup.exe.
3. Follow the prompts provided by the setup wizard. Once setup is complete, a window containing several icons displays.

Set up MWA to communicate with servers

1. Launch MWA by double-clicking the RomPilot MWA icon.
2. Specify a directory path, either by entering one or by accepting the default. This message displays:

   ```
   Do you want to create a new User Verification Phrase?
   ```

3. Click OK. The program prompts you to enter a Pass-Phrase.
4. Enter and verify the pass-phrase you created during server configuration.

   The Management Workstation Application window displays, where you can configure individual servers.

Link the client with server(s)

1. Select New from the File menu.
2. Enter the server's IP address.

   If you selected a DHCP server during server configuration, you do not have a fixed IP address for this server. To complete this field, enter a "dummy" IP address, such as "10.10.100.1".

   The Server Properties screen displays.
3. Enter the server's name. Use the name you created during server configuration.
4. Specify a Pass Phrase:

   A. Click the Enter Pass Phrase button.

   B. Enter and verify a pass-phrase. Use the same pass-phrase you created during server configuration.

   The Server Properties window displays.
5. Press OK to accept this server's information and to add this server to the client's database.

Repeat these steps for each server.

K Re-programming the flash chip

This appendix details how to update or recover your system BIOS, Flash Boot Device (FBD), and Boot Block. You accomplish this by re-programming all or part of the EPC-1316's flash chip.

When reading this file online, you can immediately view information about any topic by placing the mouse cursor over a task and clicking.

Task	Page
About the flash chip	151
About re-programming the flash chip	152
Before you begin	153
Creating a Flash Boot diskette	155
Using phlash.exe to re-program the flash chip	157
Using BIOS configuration options to re-program the flash chip	158
Using jumpers to re-program the flash chip	159

About the flash chip

The EPC-1316 flash chip contains these major sections:

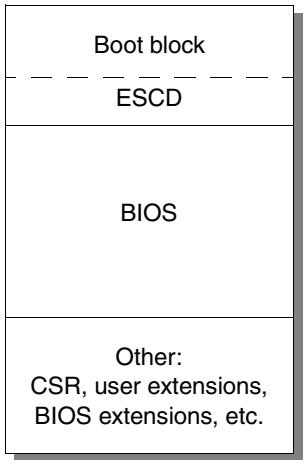


Figure K-1. Flash chip configuration

- **Boot block**: A 16 KB, hardware-write-protected area that contains the Boot Block program. This program:
  - Completes minimal hardware setup, including checking for conditions that require re-programming the flash chip.
  - Initiates a re-flash if conditions warrant. When initiating a re-flash, this program looks for the file necessary to re-flash (described in *Creating a Flash Boot diskette* on page 155) in a floppy diskette drive.
  - Passes control to the BIOS program.
- **BIOS**: Initializes the hardware and finds a device from which to bootload. The BIOS menus enable you to change the system's behavior and configuration. For details about the EPC-1316 BIOS, see *Chapter 3, BIOS configuration*.
- **Other**: The remaining reprogrammable area contains various BIOS data structures.

About re-programming the flash chip

On rare occasions, part or all of the flash chip contents may require replacement.

Use extreme caution when re-programming the flash chip. The Boot Block rarely changes and should not require re-programming.

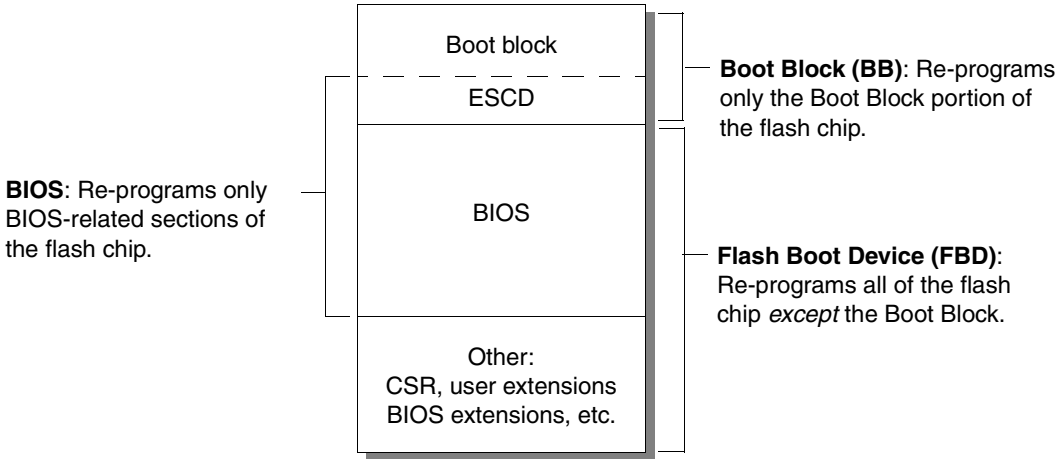

Boot block
ESCD
BIOS
Other:
CSR, user extensions
BIOS extensions, etc.
Boot Block (BB): Re-programs only the Boot Block portion of the flash chip.
BIOS: Re-programs only BIOS-related sections of the flash chip.
Flash Boot Device (FBD): Re-programs all of the flash chip *except* the Boot Block.

Figure K-2. Flash chip re-programming coverage

You can set options that force re-programming upon reboot via one of these:

- **phflash program**: Re-programs the flash chip from a DOS command prompt.
- **BIOS configuration program options**: This is the easiest and fastest way to re-program the flash chip, provided your system is connected to a floppy drive.
- **Force recovery jumper**: This technique is useful if a keyboard and monitor are not available.

When re-programming the flash chip, follow this process. The rest of this chapter includes detailed instructions for each task:

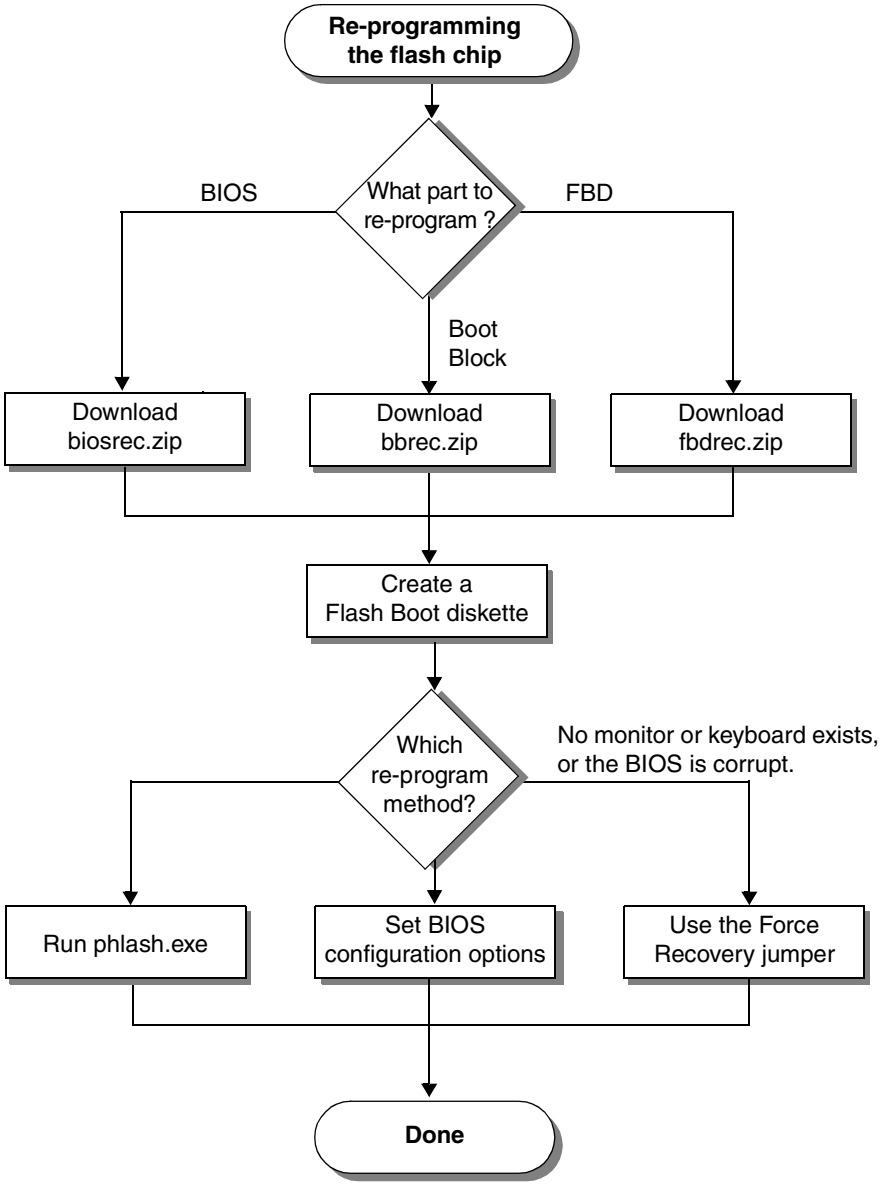


Figure K-3. Flash chip re-programming process flow

Before you begin

- Ensure that you have the following:
  - Minimum 2 MB of DRAM to run the re-flash program
  - A 3.5" 1.44 MB floppy diskette drive attached to or installed in the system
  - A floppy diskette

- Access to the RadiSys web site.

  To access the RadiSys web site, enter this URL in your web browser:
  `http://www.radisys.com`

- Decide which portion of your flash chip to re-program:
  - **BIOS**: Re-program the BIOS to fix bugs, add new features, and replace a corrupted BIOS. This is the portion of the flash chip most frequently updated. You can perform this update whether or not the BIOS can boot the system.
  - **FBD**: Re-program the FBD when you need to re-program all of the flash chip except the Boot Block. Your flash chip may require this type of update if code or data structures outside the BIOS area require an update. You can perform this update whether or not the BIOS or FBD can boot the system.
  - **Boot Block**: Re-program only the Boot Block. You will perform this type of update rarely, if ever.

    If the Boot Block is corrupt and not executable, return the EPC-1316 to the factory for repair. For information about returning items to RadiSys, see the RadiSys web site.

- Decide which re-programming process to use:
  - **phlash program**: Use this method to re-program the BIOS or FBD from the DOS command line. RadiSys recommends this as the method that provides the most feedback during the re-programming process.

    This process cannot be performed in a non-DOS OS (for example: Windows NT, QNX, or LINUX).

  - **BIOS configuration program options**: Use this method if the existing BIOS runs. RadiSys recommends this as the simplest method.

    Select this process if your system runs a non-DOS OS (for example: Windows NT, QNX, or LINUX).

  - **Force recovery jumper**: Use this method when you have physical access to the board, but no keyboard or monitor, or when the BIOS is corrupt.

Creating a Flash Boot diskette

Re-programming the flash chip requires a Flash Boot diskette that contains both code to perform the task and data to place in the chip.

To create the Flash Boot diskette:

1. Locate the appropriate file from the RadiSys web site and download it to your computer:
   - **biosrec.zip**: Select this file when you want to re-program only the BIOS-related files.
   - **fbdrec.zip**: Select this file when you want to re-program all of the flash chip except the Boot Block.
   - **bbrec.zip**: Select this file when you plan to re-program only the Boot Block.

   Use extreme caution when re-programming the Boot Block. A BIOS boot block rarely changes and should not require re-programming.

2. Unzip the contents to a directory on your hard drive.

   When unzipped, verify that these files required to re-program the flash chip are copied successfully to your hard drive:

Filename	Description
readme.txt	Describes the transmittal and includes instructions and issues that arose too late to include in other documentation
bios.rom	A binary file that contains the BIOS image and Boot Block.
crisboot.bin	The boot sector image.
crisdisk.bat	A batch file that creates the Flash Boot diskette.
makeboot.exe	Creates the custom boot sector on the diskette.
phlash.exe	The program that re-programs the flash chip using data from the other files.
platform.bin	A file that describes the flash chip configuration, and identifies which blocks to erase and re-program.
minidos.sys	A file that takes the place of DOS on the flash boot diskette.

3. Run crisdisk.bat. This program runs on MS-DOS, Windows 95, Windows 98, or Windows NT. Select this program if your system runs only MS-DOS or if you prefer to respond to command line prompts.

   If your Flash Diskette contains only one of these programs, you must use that program to create the Flash Boot diskette.

   Insert a blank, formatted, 1.44MB floppy diskette into the system drive, then complete tasks as prompted by the program.

Now that you have created a Flash Boot diskette, re-flash your system using the directions for the re-flash method you want to use:

Method	Page
Using phlash.exe to re-program the flash chip	157
Using BIOS configuration options to re-program the flash chip	158
Using jumpers to re-program the flash chip	159

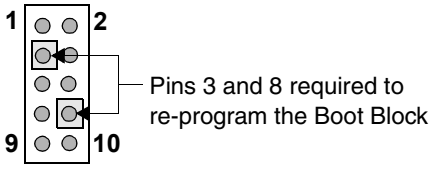
Using phlash.exe to re-program the flash chip

1. If you plan to include the Boot Block when re-programming the flash chip, connect the Boot Block Write Enable pins:

   Do not install this jumper unless a Boot Block update is required. A BIOS boot block rarely changes and seldom, if ever, requires re-programming.

   A. Turn system power off, then remove the EPC-1316 from the CompactPCI chassis.

   B. Connect these pins:



2. Boot system into MS-DOS with no memory managers running.

   If your system runs Windows 95, or Windows 98, press the F8 key during boot to enter DOS.

3. Insert the Flash Boot diskette into the floppy drive.

   For detailed information about creating a Flash Boot diskette, see *Before you begin* on page 153

4. Start the re-programming process by entering the drive the floppy disk is in followed by the phlash command. For example:

   ```
   a:\phlash
   ```

   When finished, the phlash program displays a message.

5. Remove the Flash Boot diskette from the drive when the drive stops accessing the disk.

   Determining when disk access has stopped is difficult. Typically, the disk drive makes anywhere from 15–30 accesses, then stops making access sounds for about 5 seconds. At this time you should remove the disk.

   If disk access sounds resume, the re-program process is repeating. Wait until disk access again stops, then remove the disk.

6. If you re-programmed the Boot Block, remove the Boot Block write enable jumper and return the system to normal operation:

   A. Turn system power off.

   B. Locate the BIOS configuration jumper block and disconnect the Boot Block Write Enable pins.

   C. Replace the EPC-1316 in the CompactPCI chassis.

   D. Power up the EPC-1316.

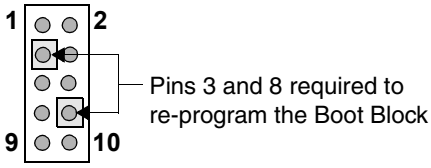
Using BIOS configuration options to re-program the flash chip

1. If you plan to re-program the Boot Block, connect the Boot Block Write Enable pins:

   Do not install this jumper unless a Boot Block update is required. A BIOS boot block rarely changes and seldom, if ever, requires re-programming.

   A. Turn system power off, then remove the EPC-1316 from the CompactPCI chassis.

   B. Connect these pins:

   C. Power up the EPC-1316 and run the BIOS configuration program.

2. Select the Exit and Update BIOS option in the BIOS configuration program's Exit menu. The BIOS configuration program instructs the BIOS to run an update (re-program the flash chip) upon reboot, then terminates and reboots the system.

3. Re-program the flash chip:

   A. Insert the Flash Boot diskette into the floppy drive.

   The phlash.exe program automatically runs and re-programs the flash chip.

   No video displays during this type of update.

   B. Remove the Flash Boot diskette from the drive when the drive stops accessing the disk.

4. If you re-programmed the Boot Block, remove the Boot Block write enable jumper and return the system to normal operation:

   A. Turn system power off.

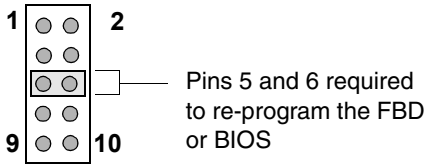
   B. Locate the BIOS configuration jumper block and disconnect the Boot Block Write Enable pins.

   C. Replace the EPC-1316 in the CompactPCI chassis.

   D. Power up the EPC-1316.

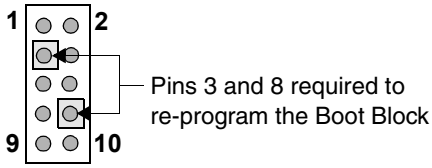
Using jumpers to re-program the flash chip

1. Install the force recovery jumper:
   A. Turn system power off, then remove the EPC-1316 from the CompactPCI chassis.
   B. Locate the BIOS configuration jumper block and connect the appropriate pins:
      i. To re-program the BIOS or the FBD, connect the Force BIOS Recovery pins:



      ii. To re-program the Boot Block, you must also connect the Boot Block Write Enable pins:

Do not install this jumper unless a Boot Block update is required. A BIOS boot block rarely changes and seldom, if ever, requires re-programming.



2. Re-program the flash chip:
   A. Insert the Flash Boot diskette into the floppy drive.
   B. Power up the EPC-1316. The phlash.exe program automatically runs and re-programs the flash chip.
   C. Remove the Flash Boot diskette from the drive when the drive stops accessing the disk.

Determining when disk access has stopped is difficult. Typically, the disk drive makes anywhere from 15–30 accesses, then stops making access sounds for about 5 seconds. At this time you should remove the disk.

If disk access sounds resume, the re-program process is repeating. Wait until disk access again stops, then remove the disk.

3. Remove the force recovery jumper and return the system to normal operation:
   A. Turn system power off.
   B. Locate the BIOS configuration jumper block and disconnect the Force BIOS Recovery pins and, if you connected them, the Boot Block Write Enable pins.
   C. Replace the EPC-1316 in the CompactPCI chassis.
   D. Power up the EPC-1316.

L Glossary

Access Time: A factor in measurement of a memory storage device's operating speed. It is the amount of time required to perform a read operation. More specifically, it is the period of time between which the memory receives a read command signal and the time when the requested data becomes available to the system data bus.

Address: A number that identifies the location of a word in memory. Each word in a memory storage device or system has a unique address. Addresses are always specified as a binary number, although octal, hexadecimal, and decimal numbers are often used for convenience.

APM: Advanced Power Management. A software interface specification that allows operating system device drivers to control the power management functionality of a PC.

ANSI: American National Standards Institute. An organization dedicated to advancement of national standards related to product manufacturing.

ATA: AT Bus Attachment. An interface definition for PC peripherals. See IDE.

Autotype: A convenient method of IDE device detection whereby the system BIOS queries the IDE device to obtain operational parameters. If the device supports autotype, this information is passed to the BIOS where it is used to automatically configure the drive controller.

BIOS: Basic Input/Output System. Firmware in a PC-compatible computer that runs when the computer is powered up. The BIOS initializes the computer hardware, allows the user to configure the hardware, boots the operating system, and provides standard mechanisms that the operating system can use to access the PC's peripheral devices.

BDA: BIOS Data Area. BIOS Data Area. A 256 byte block of DRAM starting at address 400H that contains data initialized and used by the System BIOS detailing the system configuration and errors encountered during POST.

BIOS Extension: An object code module that is typically integrated into the FBD or placed into a ROM that is accessible on the peripheral bus (PCI, ISA, etc.) in the address range 0C0000h through 0DFFFFh. BIOS extensions have a pre-defined header format and contain code that is used to extend the capabilities of the System BIOS.

BIOS Image: Information contained in the flash boot device in binary file format consisting of initialization data, setup configuration data, diagnostic sequences, and other instructions necessary to start up a computer and prepare it to load an operating system.

BIOS Recovery: A process whereby an existing, corrupt BIOS image in the flash boot device is overwritten with a new image. Also referred to as a flash recovery.

BIOS Update: A process whereby an existing, uncorrupted BIOS image in the flash boot device is overwritten with a new image. Also referred to as a flash update.

Bit: A binary digit. Boot: The process of starting a computer and loading the operating system from a powered down state (cold boot) or after a computer reset (warm boot). Before the operating system loads, the computer performs a general hardware initialization and resets internal registers.

Boot Block: A write-protected 16KB section of the flash boot device located at physical address FFFFC000h to FFFFFFFFh which contains code to perform rudimentary hardware initialization at system power up. The boot block also contains code to recover the BIOS via floppy disk.

Boot Device: The storage device from which the computer boots the operating system.

Boot Sequence: The order in which a computer searches external storage devices for an operating system to boot. The boot device must be the first in the boot sequence.

Byte: A group of 8 bits.

CPU: Central Processing Unit. A semiconductor device which performs the processing of data in a computer. The CPU, also referred to as the microprocessor, consists of an arithmetic/logic unit to perform the data processing, and a control unit which provides timing and control signals necessary to execute instructions in a program.

Chipset: One or more integrated circuits that, along with a CPU, memory, and other peripherals, implements an IBM PC-AT compatible computer. The chipset typically implements a DRAM controller, bus, interface logic, and PC peripheral devices.

CAS: Column Address Strobe. An input signal from the DRAM controller to an internal DRAM latch register specifying the column at which to read or write data. The DRAM requires a column address and a row address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of column addresses and row addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

COM Port: A bi-directional serial communication port which implements the RS-232 specification.

CMOS: Complimentary Metal Oxide Semiconductor. A fast, low power semiconductor RAM used to store system configuration data.

Conventional Memory: The first 640 KB of a computer's total memory capacity. If a computer has no extended memory, conventional memory equals the total memory capacity. In typical computer systems, conventional memory can contain BIOS data, the operating system, applications, application data, and terminate and stay resident (TSR) programs. Also called system memory.

CSR: CMOS Save and Restore. A System BIOS feature that allows the user to backup the contents of CMOS RAM (contained within the real time clock) to

the BIOS Flash device to be restored later if necessary (such as when the real time clock battery dies).

CHS: Cylinders/Heads/Sectors. A specification of disk drive operating parameters consisting of the number of disk cylinders, disk drive read/write heads, and disk sectors.

Default: The state of all user-changeable hardware and software settings as they are originally configured before any changes are made.

DOS: Disk Operating System. One or more programs which allow a computer to use a disk drive as an external storage device. These programs manage storage and retrieval of data to and from the disk and interpret commands from the computer operator.

Driver: A software component of the operating system which directs the computer interface with a hardware device. The software interface to the driver is standardized such that application software calling the driver requires no specific operational information about the hardware device.

DIP: Dual In-Line Package. A semiconductor package configuration consisting of a rectangular plastic case with two rows of pins, one row on each lengthwise side.

DRAM.: Dynamic Random Access Memory. Semiconductor RAM memory devices in which the stored data does not remain permanently stored, even with the power applied, unless the data are periodically rewritten into memory during a refresh operation.

EEPROM: Electrically Erasable Programmable ROM. Specifically, those EPROMs which may be erased electrically as compared to other erasing methods.

Error Checking and Correction: A feature of the T2 chipset that enables it to detect single or multi-bit errors in DRAM reads and correct single bit errors. This feature requires that all banks of DRAM use x36 (parity) SO DIMMs.

ECP: Extended Capabilities Port. An enhancement of the standard PC parallel port that allows high speed bi-directional data transfers and other features.

EDO: Extended Data Out. A type of DRAM that allows higher memory system performance since the data pins are still driven when ~CAS is de-asserted. This allows the next DRAM address to be presented to the device sooner than with Fast Page Mode DRAM.

Extended Memory: The RAM address space, in a computer so equipped, above the 1 MB level.

ESCD: Extended System Configuration Data. A block of nonvolatile memory that stores information on the devices found and configured by the Plug and Play BIOS.

EXP-FDM: Expansion Floppy Disk Module. A Radisys product which enables VME users to add an external floppy drive into a VME chassis without external power cables.

External Device: A peripheral or other device connected to the computer from an external location via an interface cable.

FPM: Fast Page Mode. A "standard" type of DRAM that is lower performance than EDO.

Fixed Disk: A hard disk drive or other data storage device having no removable storage medium. Fixed disk storage devices use inflexible disk media and are sealed to prevent data loss due to media surface contamination. Fixed disks generally provide the most storage space for a given cost when compared to semiconductor, tape, and other popular mass storage technologies.

FPGA: Field Programmable Gate Array. A large, general-purpose logic device that is programmed at power-up to perform specific logic functions.

FBD: Flash Boot Device. A flash memory device containing the computer's BIOS. In the EPC-1316, a 1 MByte Intel 28F800B5 semiconductor flash memory containing the system and video BIOS images, the BIOS initializing code and the recovery code which allows self hosted reflashing.

Flash Memory: A fast EEPROM semiconductor memory typically used to store firmware such as the computer BIOS. Flash memory also finds general application where a semiconductor non-volatile storage device is required.

Flash Recovery: See BIOS Recovery.

Flash Update: See BIOS Update.

Force Update: See BIOS Recovery.

GB or GByte: Gigabyte. Approximately one billion (US) or one thousand million (Great Britain) bytes. 2^30 = 1,073,741,824 bytes exactly.

Hang: A condition where the system microprocessor suspends processing operations due to an anomaly in the data or an illegal instruction.

Header: A mechanical pin and sleeve style connector on a circuit board. The header may exist in either a male or female configuration. For example, a male header has a number and pattern of pins which corresponds to the number and pattern of sleeves on a female header plug.

h: Hexadecimal. A base 16 numbering system using numeric symbols 0 through 9 plus alpha characters A, B, C, D, E, and F as the 16 digit symbols. Digits A through F are equivalent to the decimal values 10 through 15.

Host Bus: The address/data bus that connects the CPU and the chipset.

ISA: Industry Standard Architecture. A popular microcomputer expansion bus architecture standard. The ISA standard originated with the IBM PC when the system bus was expanded to accept peripheral cards.

I/O: Input/Output. The communication interface between system components and between the system and connected peripherals.

IDE: Integrated Drive Electronics. A hard disk drive/controller interface standard. IDE drives contain the controller circuitry at the drive itself, as compared to the location of this circuitry on the computer motherboard in non-IDE systems. IDE drives typically connect to the system bus with a simple adapter card containing a minimum of on-board logic.

IRDA or IrDA: Infra-red Data Association. A specification for high-speed data communication using infrared drivers and receivers for short-range wireless data transmission.

INT: Interrupt Request. A software-generated interrupt request.

IRQ: Interrupt Request. In ISAbus systems, a microprocessor input from the control bus used by I/O devices to interrupt execution of the current program and cause the microprocessor to jump to a special program called the interrupt service routine. The microprocessor executes this special program, which normally involves servicing the interrupting device. When the interrupt service routine is completed, the microprocessor resumes execution of the program it was working on before the interruption occurred.

ISR: Interrupt Service Routine. A program executed by the microprocessor upon receipt of an interrupt request from an I/O device and containing instructions for servicing of the device.

Jumper: A set of male connector pins on a circuit board over which can be placed coupling devices to electrically connect pairs of the pins. By electrically connecting different pins, a circuit board can be configured to function in predictable ways to suit different applications.

KB or KByte: Kilobyte. Approximately one thousand bytes. 2^{10} = 1024 bytes exactly.

Logical Address: The memory-mapped location of a segment after application of the address offset to the physical address.

LBA: Logical Block Addressing. A method the system BIOS uses to reference hard disk data as logical blocks, with each block having a specific location on the disk. LBA differs from the CHS reference method in that the BIOS requires no information relating to disk cylinders, heads, or sectors. LBA can be used only on hard disk drives designed to support it.

MB or MByte: Megabyte. Approximately one million bytes. 2^20 = 1,048,576 bytes exactly.

Memory: A designated system area to which data can be stored and from which data can be retrieved. A typical computer system has more than one memory area. See Conventional Memory and Extended Memory.

Memory shadowing: Copying information from an extension ROM into DRAM and accessing it in this alternate memory location.

Offset: The difference in location of memory-mapped data between the physical address and the logical address.

Operating System: See DOS.

PMC: PCI Mezzanine Card. A new standard form factor for PCI add-in modules. PMCs mate with their respective connectors on the motherboard and are secured with screws.

PCI: Peripheral Connect Interface. A popular microcomputer bus architecture standard.

Peripheral Device: An external device connected to the system for the purpose of transferring data into or out of the system.

PC/AT: Personal Computer/Advanced Technology. A popular computer design first introduced by IBM in the early 1980s.

PS/2: Personal System 2. Computers designed with IBM's proprietary bus architecture known as Micro Channel.

PLL: Phase-Locked Loop. A semiconductor device which functions as an electronic feedback control system to maintain a closely regulated output frequency from an unregulated input frequency. The typical PLL consists of an internal phase comparator or detector, a low pass filter, and a voltage controlled oscillator which function together to capture and lock onto an input frequency. When locked onto the input frequency, the PLL can maintain a stable, regulated output frequency (within bounds) despite frequency variance at the input.

Physical Address: The address or location in memory where data is stored before it is moved as memory remapping occurs. The physical address is that which appears on the computer's address bus when the CPU requests data from a memory address. When remapping occurs, the data can be moved to a different memory location or logical address.

Pinout: A diagram or table describing the location and function of pins on an electrical connector.

PQFP: Plastic Quad Flat Pack. A popular package design for integrated circuits of high complexity.

POST: Power On Self Test. A diagnostic routine which a computer runs at power up. Along with other testing functions, this comprehensive test initializes the system chipset and hardware, resets registers and flags, performs ROM checksums, and checks disk drive devices and the keyboard interface.

Program: A set of instructions a computer follows to perform specific functions relative to user need or system requirements. In a broad sense, a program is also referred to as a software application, which can actually contain many related, individual programs.

PAL: Programmable Array Logic. A semiconductor programmable ROM which accepts customized logic gate programming to produce a desired sum-of-products output function.

RAM: Random Access Memory. Memory in which the actual physical location of a memory word has no effect on how long it takes to read from or write to that location. In other words, the access time is the same for any address in memory. Most semiconductor memories are RAM.

ROM: Read Only Memory. A broad class of semiconductor memories designed for applications where the ratio of read operations to write operations is very high. Technically, a ROM can be written to (programmed) only once, and this operation is normally performed at the factory. Thereafter, information can be read from the memory indefinitely.

Real Mode: The operational mode of Intelx86 CPUs that uses a segmented, offset memory addressing method. These CPUs can address 1 MB of memory using real mode.

Real Mode Address: A memory address composed of two 16-bit values: a segment address and an offset quantity. A real mode address is constructed by shifting a segment

address 4 bits to the left and then adding the offset value. A real mode address is a physical address.

RTC: Real Time Clock. Peripheral circuitry on a computer motherboard which provides a nonvolatile time-of-day clock, an alarm, calendar, programmable interrupt, square wave generator, and a small amount of SRAM. In the EPC-1316, the RTC operates independently of the system PLL which generates the internal system clocks. The RTC is typically receives power from a small battery to retain the current time of day when the computer is powered down.

Reflashing: The process of replacing a BIOS image, in binary format, in the flash boot device.

Register: An area typically inside the microprocessor where data, addresses, instruction codes, and information on the status on various microprocessor operations are stored. Different types of registers store different types of information.

Reset: A signal delivered to the microprocessor by the control bus, which causes a halt to internal processing and resets most CPU registers to 0. The CPU then jumps to a starting address vector to begin the boot process.

RFA: Resident Flash Array. The RFA represents flash memory that is resident on the hardware platform that is utilized for OS or application purposes.

RS-232: A popular asynchronous bi-directional serial communication protocol. Among other things, the RS-232 standard defines the interface cabling and electrical characteristics, and the pin arrangement for cable connectors.

RS-485: An asynchronous bi-directional serial communication protocol using differential voltage signals. Among other things, the RS-485 standard defines the interface cabling and electrical characteristics, and the pin arrangement for cable connectors. While similar to the RS-232 standard, the RS-485 protocol allows for multiple loads and longer line lengths.

RAS: Row Address Strobe. An input signal to an internal DRAM latch register specifying the row at which to read or write data. The DRAM requires a row address and a column address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of row addresses and column addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

Segment: A section or portion of addressable memory serving to hold code, data, stack, or other information allowing more efficient memory usage in a computer system. A segment is the portion of a real mode address which specifies the fixed base address to which the offset is applied.

Serial Port: A physical connection with a computer for the purpose of serial data exchange with a peripheral device. The port requires an I/O address, a dedicated IRQ line, and a name to identify the physical connection and establish serial communication between the computer and a connected hardware device. A serial port is often referred to as a COM port.

Shadow Memory: RAM in the address range 0xC000h through 0xFFFFFh used for shadowing. Shadowing is the process of copying BIOS extensions from ROM into DRAM for the purpose of faster CPU access to the extensions when the system

requires frequent BIOS calls. Typically, system and video BIOS extensions are shadowed in DRAM to increase system performance.

SIMM: Single In-Line Memory Module. A small, rectangular circuit board on which is mounted semiconductor memory ICs.

SODIMM: Small Outline Dual Inline Memory Module. A new form factor for memory modules that is smaller and denser than SIMMs.

Standoff: A mechanical device, typically constructed of an electrically non-conductive material, used to fasten a circuit board to the bottom, top, or side of a protective enclosure.

SRAM: Static Random Access Memory. A semiconductor RAM device in which the data remains permanently stored as long as power is applied, without the need for periodically rewriting the data into memory.

Symmetrically Addressable SIMM:
A SIMM, the memory content of which is configured as two independent banks. Each 16-bit wide bank contains an equal number of rows and columns and is independently addressable by the CPU via twin row address strobe registers in the DRAM controller.

SYSCLK: ISAbus System Clock. The ~8.33MHz clock signal present on the ISAbus to which all bus transactions are synchronized.

System Memory: See Conventional Memory.

TB or TByte: Terabyte. Approximately one thousand billion (US) or one billion (Great Britain) bytes. 2^40 = 1,099,511,627,776 bytes exactly.

USB: Universal Serial Bus. A new serial data bus that is intended to eliminate the need for separate serial, parallel, mouse, keyboard, joystick, etc. ports on a PC-compatible. These ports can be conceivably replaced by a few, daisy-chained USB ports, all with identical connectors but capable of much higher throughput, upwards of 12Mbs.

UED: User Editable Drive. A feature of the EPC-1316's Phoenix NuBIOS. When a "User" type hard disk drive setting shows in the IDE Adapter Sub-Menu the BIOS queries the hard disk drive for the purpose of retrieving disk geometry. If the hard disk drive is capable of providing this information, the BIOS uses it to automatically set up the drive for use with the system.

VESA: Video Electronics Standards Association. A group of hardware and software vendors that define specifications for hardware and software interfaces for a variety of devices.

VGA: Video Graphics Adapter. A popular PC graphics controller and display adapter standard developed by IBM. The standard specifies, among other things, the resolution capabilities of the display device. Display devices meeting the VGA standard must be capable of displaying a minimum resolution of 640 horizontal pixels by 480 vertical pixels with at least 16 screen colors.

VME: VESAbus Module Europe. An open architecture backplane standard with 32 bit address and data capability

Wait State: A period of one or more microprocessor clock pulses during which the CPU suspends processing while waiting for data to be transferred to or from the system data or address buses.

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